

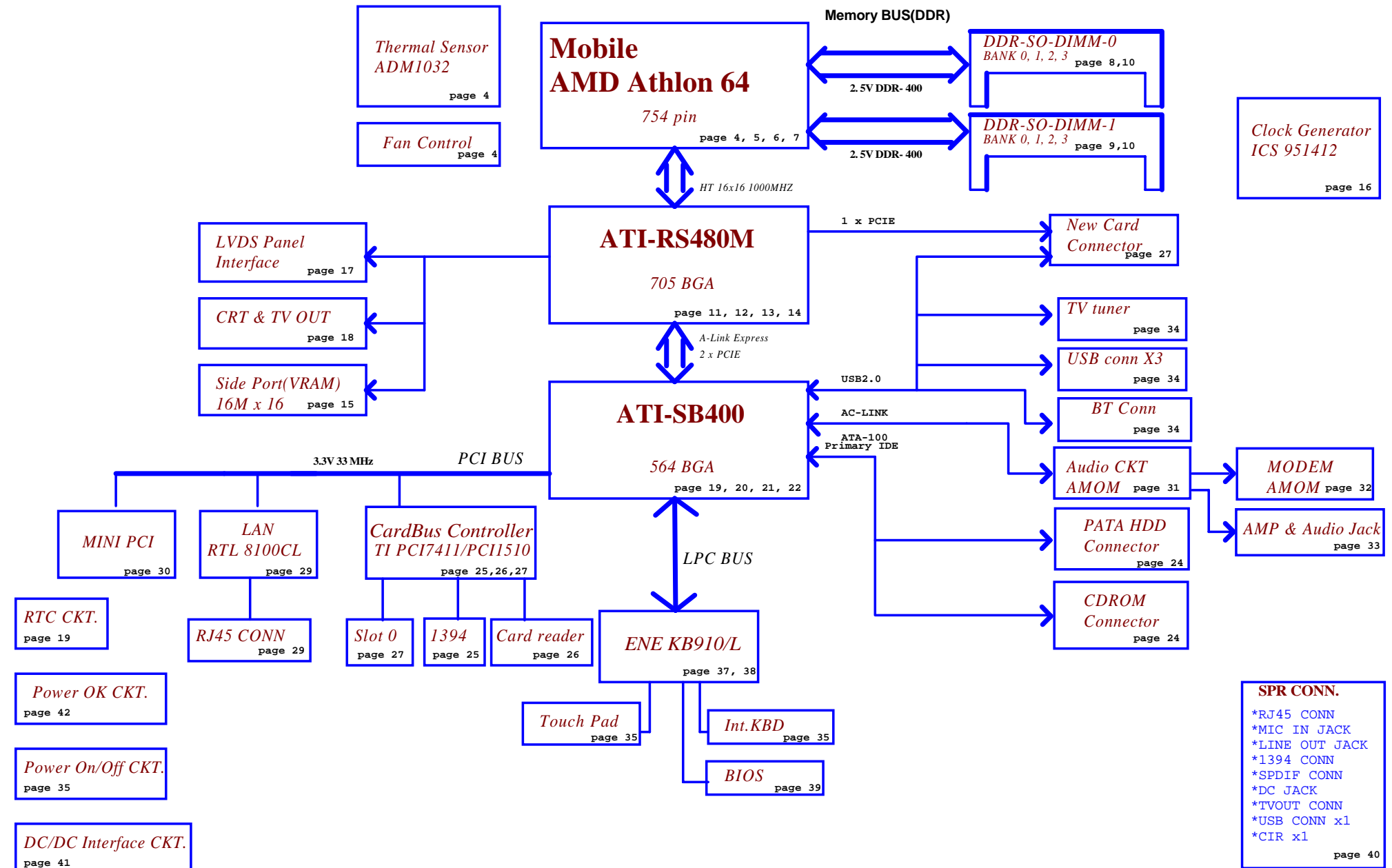
Compal confidential

Schematics Document

AMD K8 with ATI RS480M+ATI SB400

2005-08-29
REV:0.8

Security Classification		Compal Secret Data			
Issued Date	2005/03/01	Deciphered Date	2005/04/06	Title	
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				Rev	0.8



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Voltage Rails

power plane State	+12VALW +5VALW +3VALW +1.8VALW	+5V +2.5V +1.25V	+5VS +3VS +2.5VS +1.8VS +1.5VS +2.5VDDA +CPU_CORE +1.2V_HT
s0	O	O	O
s1	O	O	O
s3	O	O	X
s5 S4/AC	O	X	X
s5 S4/AC don't exist	X	X	X

O MEANS ON

X MEANS OFF

BOM STATUS :

VRAM@ ,VRAMIC@, SAMSUNG@, HYNIX@, 2HDD@ ,7411@ ,EXP@ ,17_EXP@ ,15_EXO@,CIR@ ,D@, C@, 15.4@, DOCK@, WL_LED@

45@ (for 45 level RTC battery)

HAL10 17" VRAM@ , SAMSUNG@, HYNIX@, 2HDD@ ,7411@ ,EXP@ ,17_EXP@ ,CIR@ ,D@ ,DOCK@,WL_LED@

HAL20 FF 15.4" VRAM@ , SAMSUNG@, HYNIX@, 2HDD@ ,7411@ ,EXP@ ,15_EXP@ ,CIR@ ,C@ ,DOCK@,WL_LED@, 15.4@(LED)

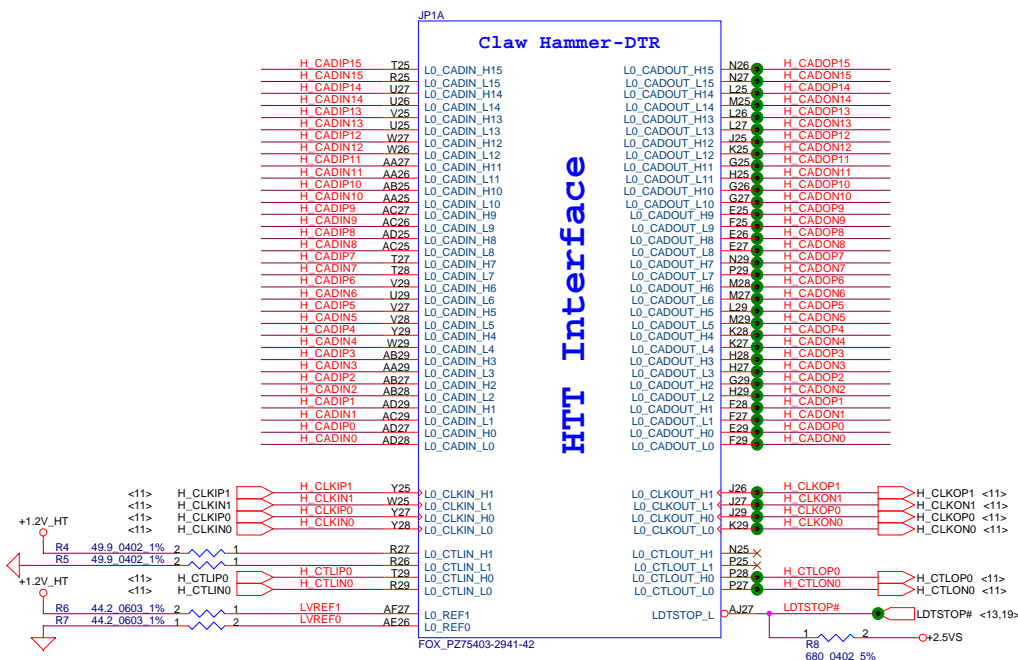
HAL20 DF 15.4" EXP@, C@ ,DOCK@ ,15.4@(LED), CIR@, WLAN@, 15_EXP@

PCI Devices

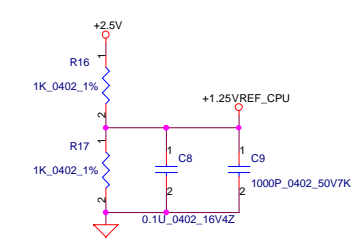
INTERNAL DEVICE	IDSEL #	REQ/GNT #	PIRQ
SMBUS			
IDE			A
LPC I/F			
PCI to PCI			
AC97 AUDIO			B
AC97 MODEM			B
OHCI#1 USB			D
OHCI#1 USB			D
EHCI USB			D
SATA#1			A
SATA#2			A

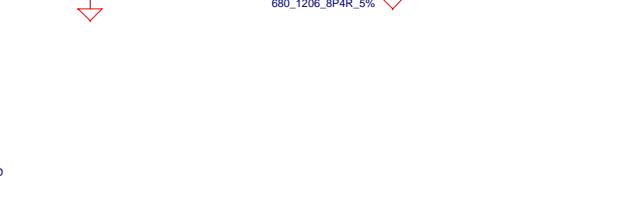
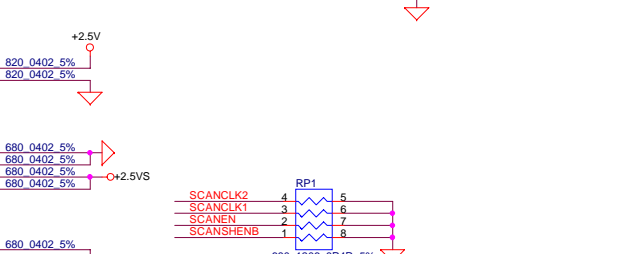
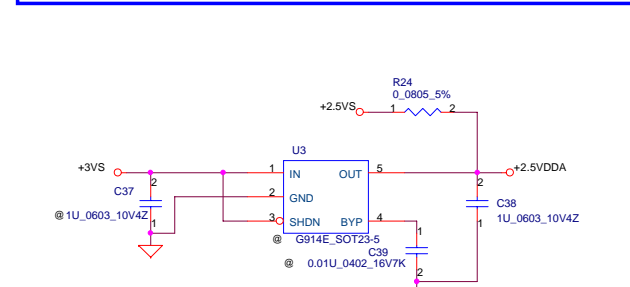
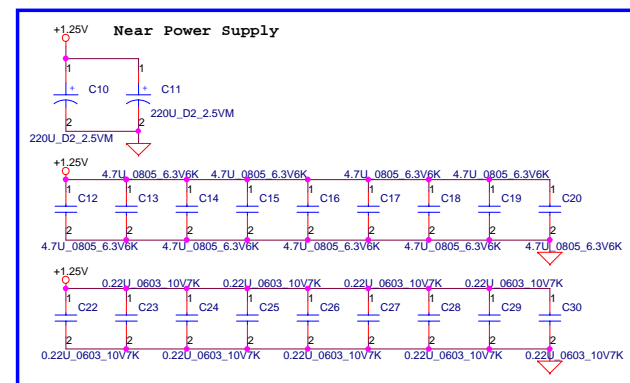
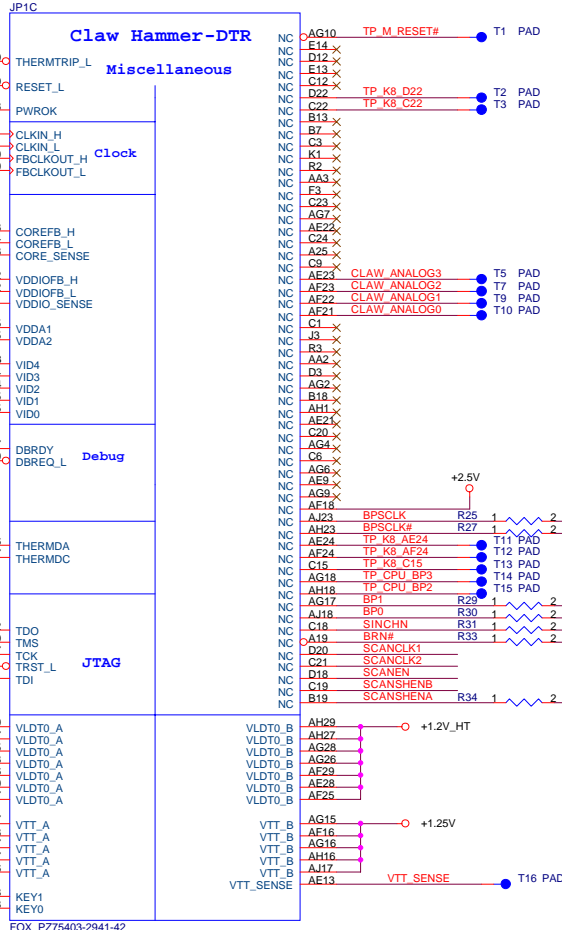
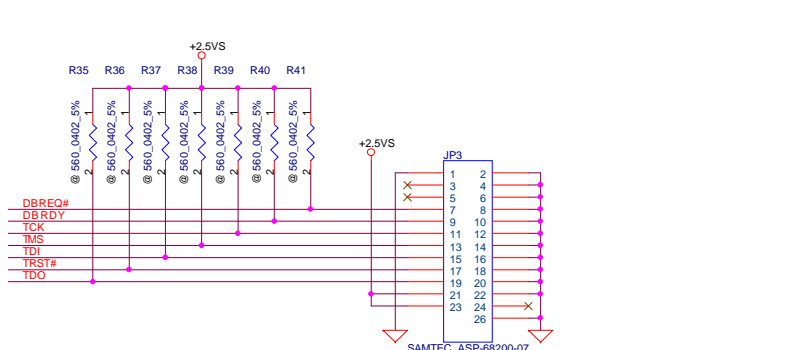
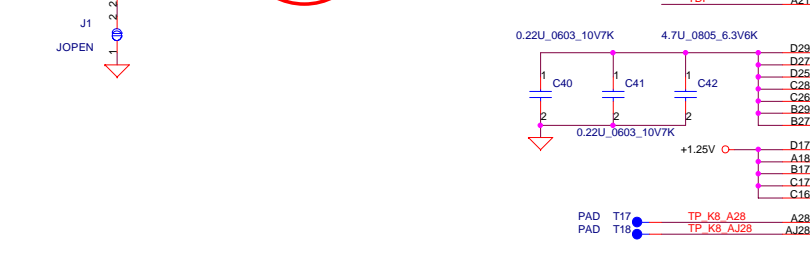
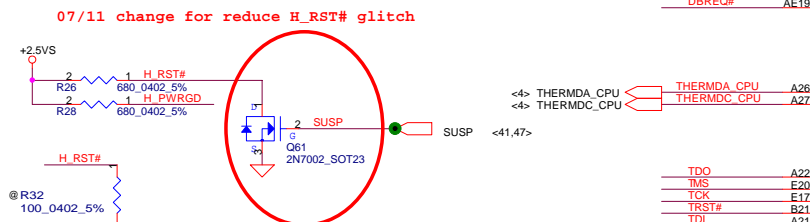
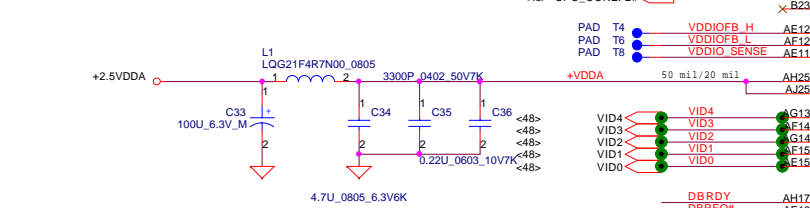
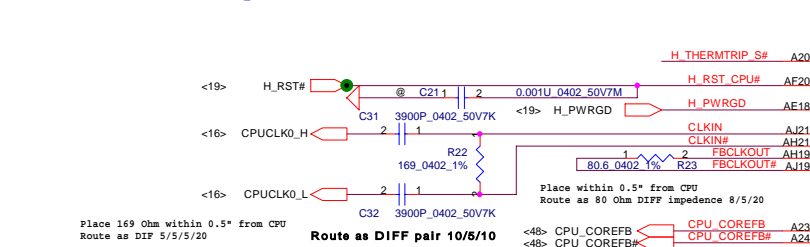
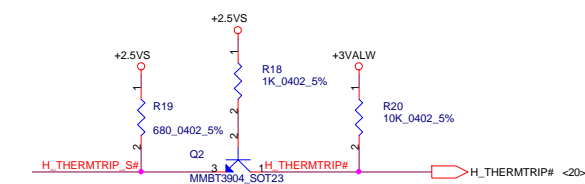
EXTERNAL			
Wireless LAN	AD18	3	F
LAN	AD22	1	G
CARD BUS & 1394	AD20	2	E,H

H_CADOP[0..15] → H_CADOP[0..15] <11>
H_CADON[0..15] → H_CADON[0..15] <11>

[illegible]

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				Size	Document Number
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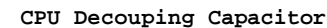




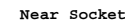
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Issued Date				Deciphered Date				Claw Hammer(MISC)			
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FOX PZ75403-2941-42



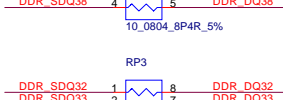
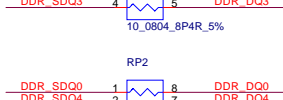
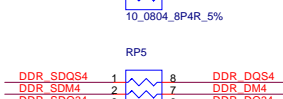
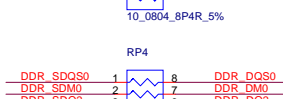
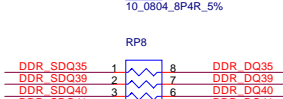
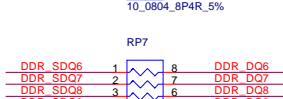
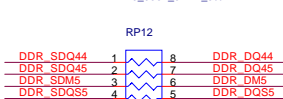
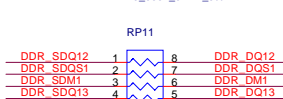
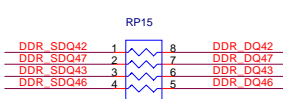
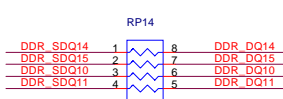
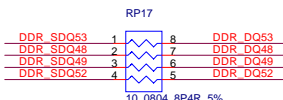
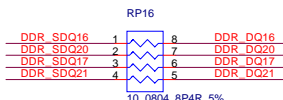
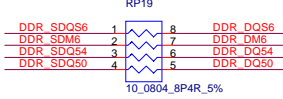
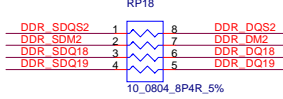
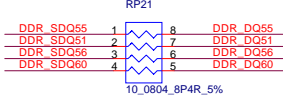
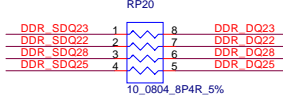
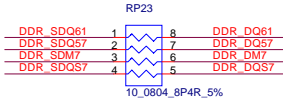
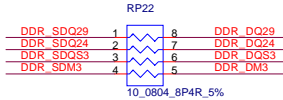
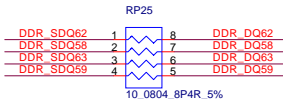
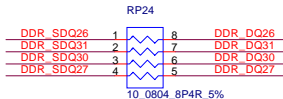
Loop Bandwidth KHz	Bulk Capacitance uF	Total ESR
20	23000	2.5m ohm (AMD)
50	9000	0.9m ohm
* 300	1500	2.5m ohm



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<-> DDR_SDQS[0..7] <-> DDR_SDQS[0..7]
<-> DDR_SDQ[0..63] <-> DDR_SDQ[0..63]
<-> DDR_SDM[0..7] <-> DDR_SDM[0..7]
<-> DDR_SMAA[0..13] <-> DDR_SMAA[0..13]

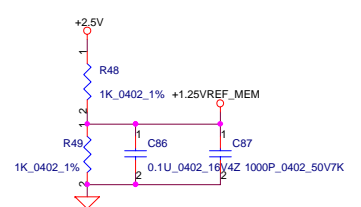
DDR_DQ[0..63] <-> DDR_DQ[0..63] <->
DDR_DQS[0..7] <-> DDR_DQS[0..7] <->
DDR_DM[0..7] <-> DDR_DM[0..7] <->



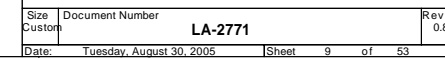
Note:
DDR_SMAA13 Recommend for AMD

Layout note
Place these resistors
close to DIMM0,
all trace length<500 mil

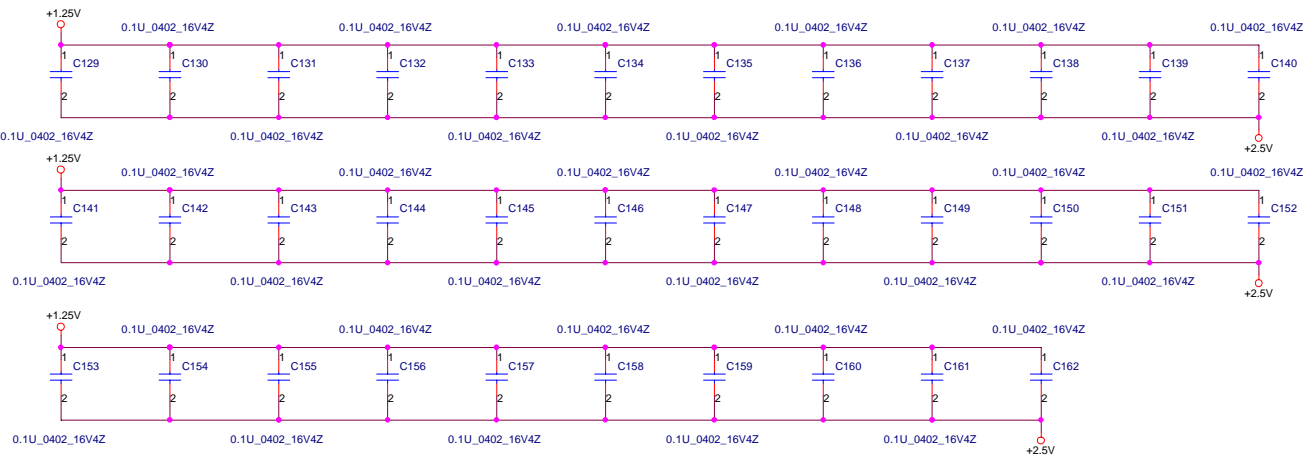
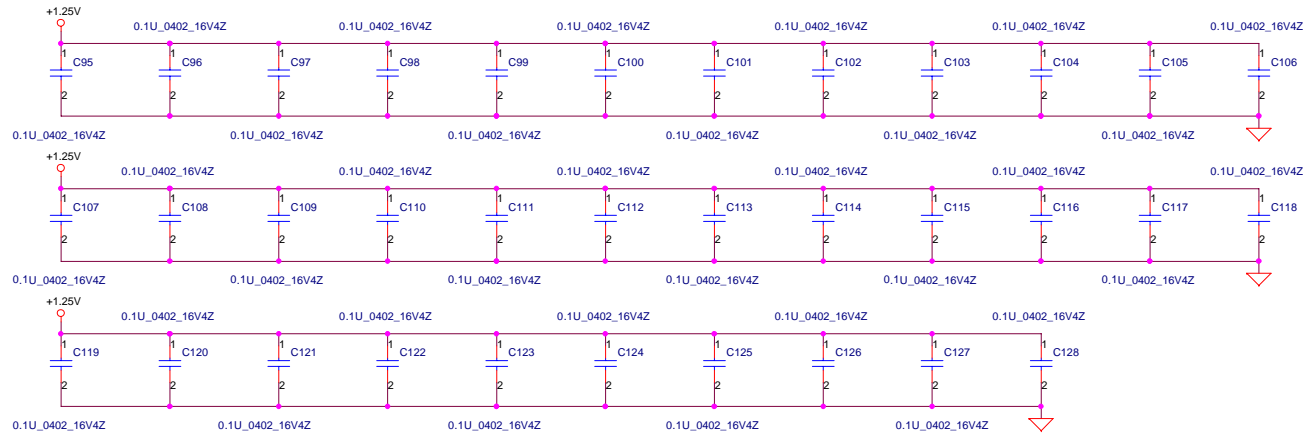
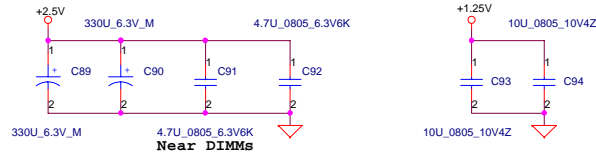
<9,16,20,28> SB_SDAT
<9,16,20,28> SB_SCLK
+3VS



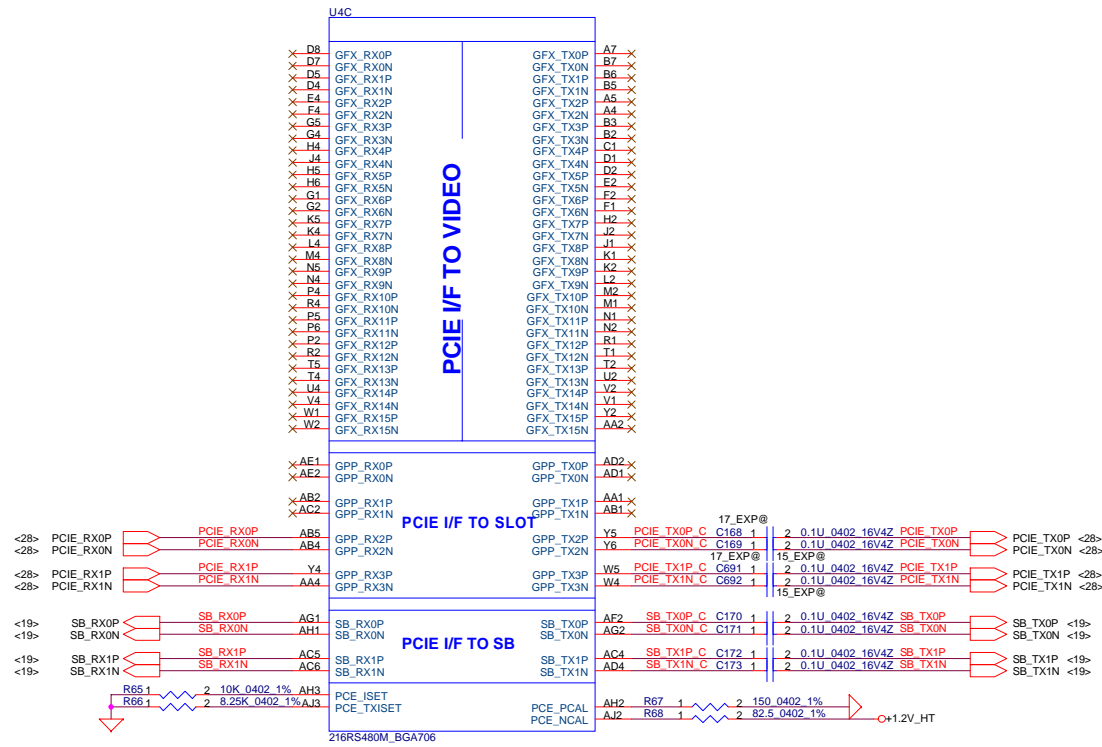
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Layout note :
Place one cap close to every 2 pull up resistors termination to +1.25V

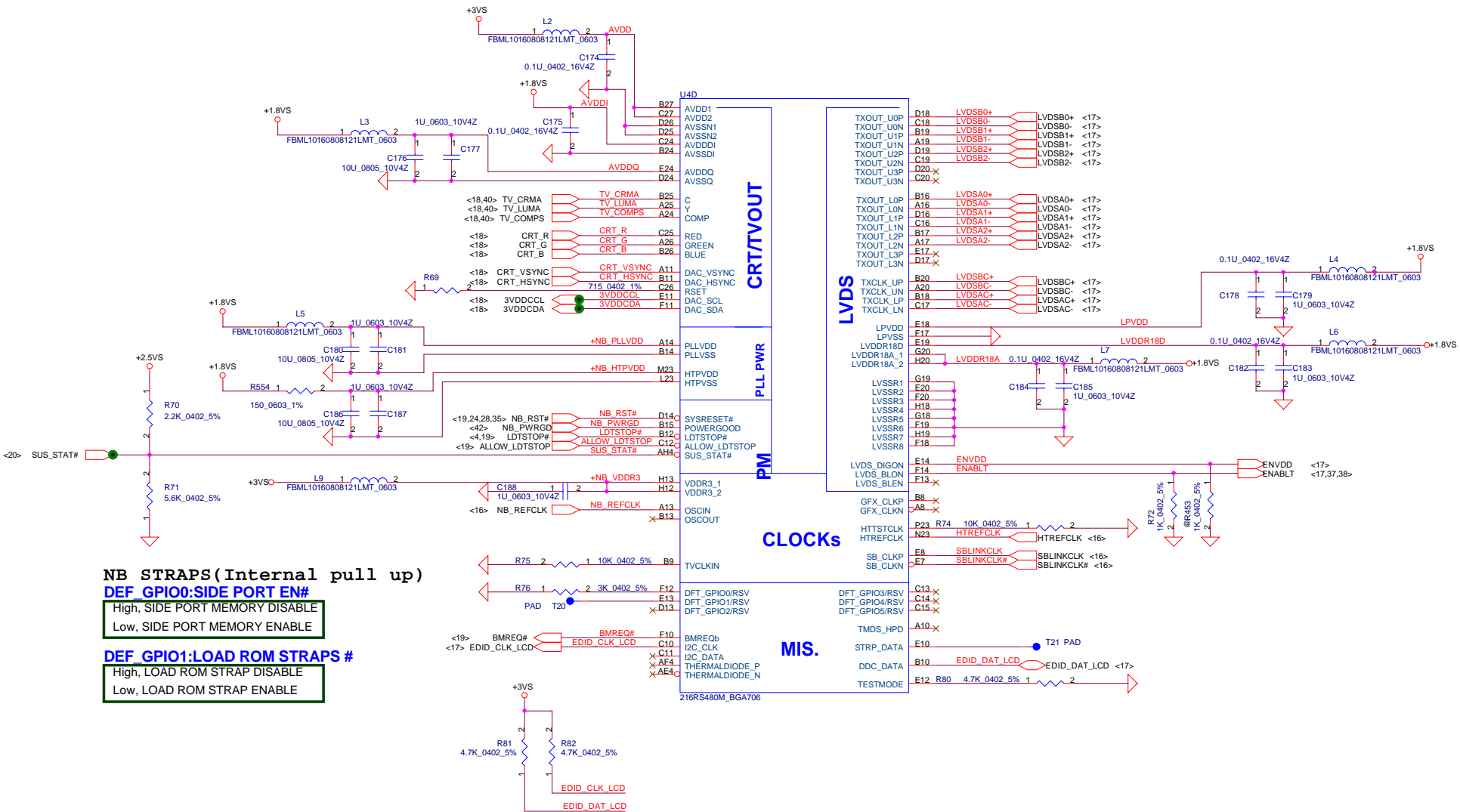


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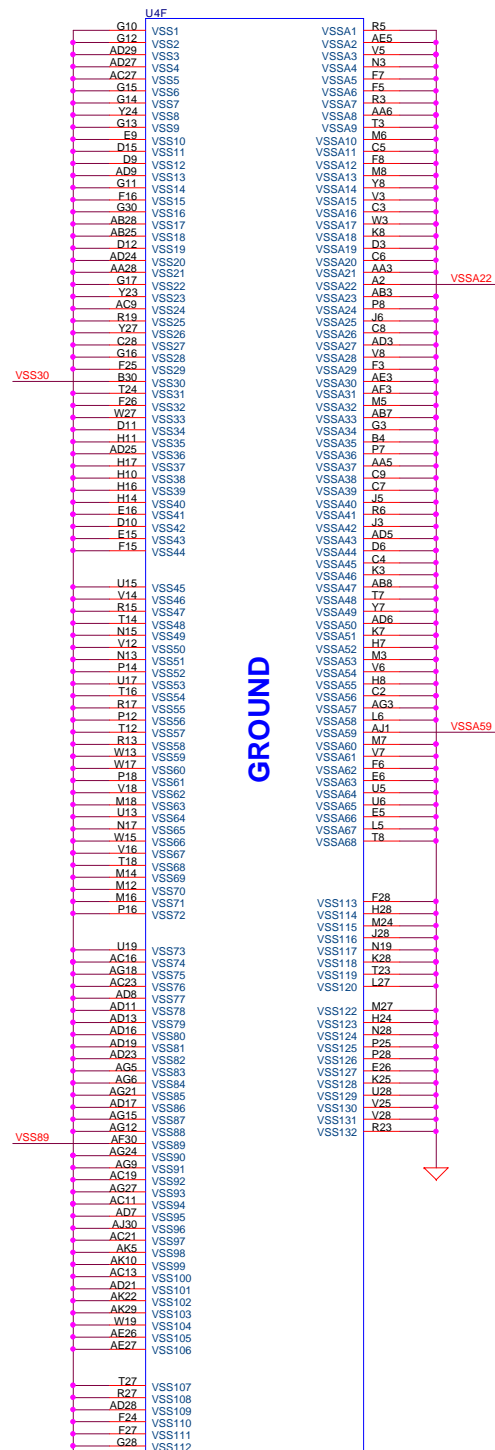


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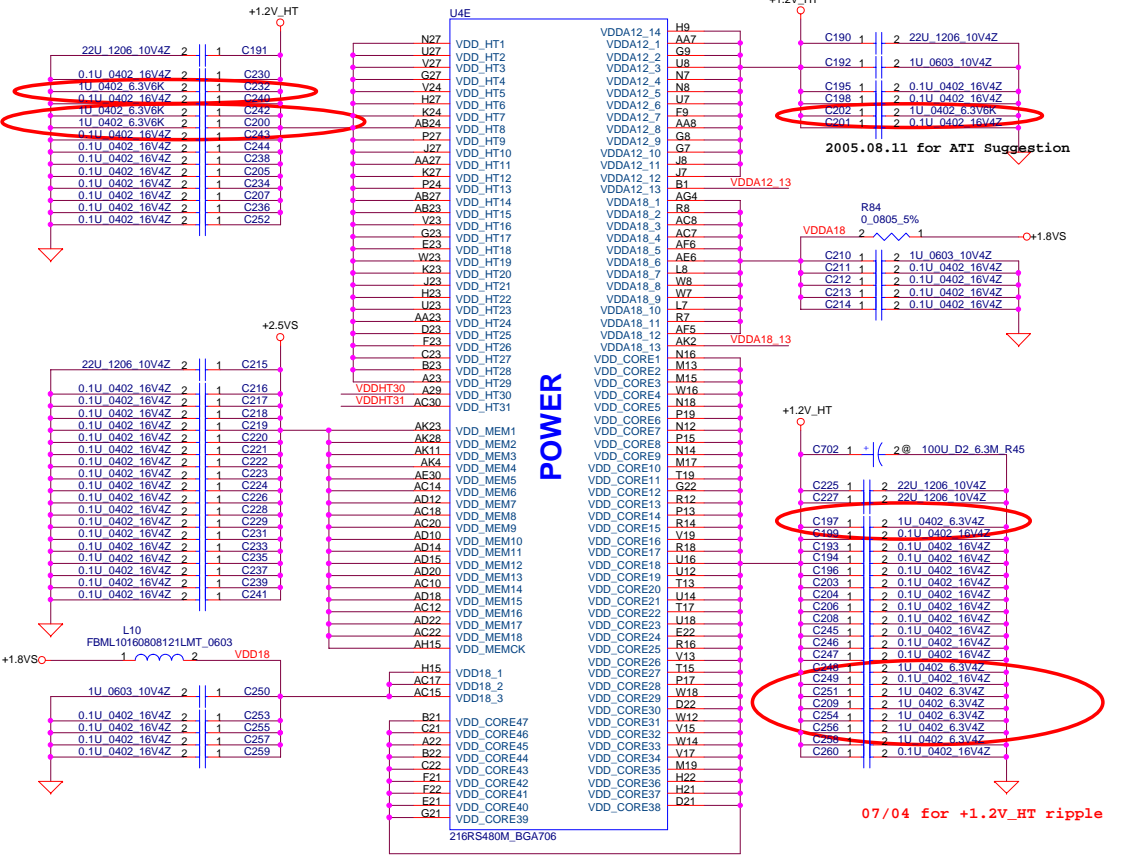
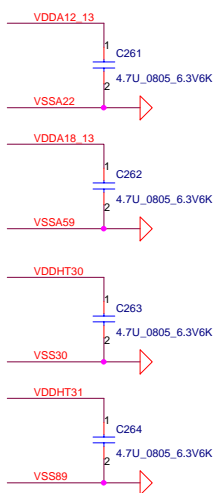
AVDD , AVDDI , AVDDQ , +NB_PLLVDD , +NB_HTPVDD
+NB_VDDR3 , LPVDD , LVDDR18D , LVDDR18A (20mils)



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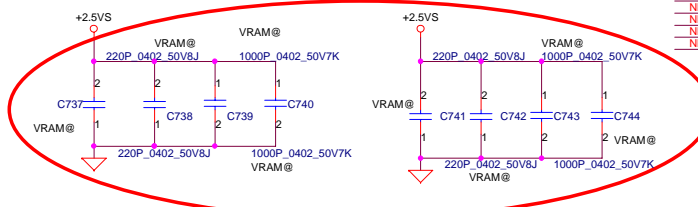
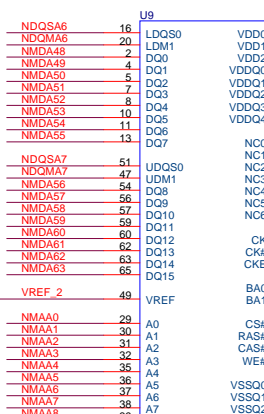
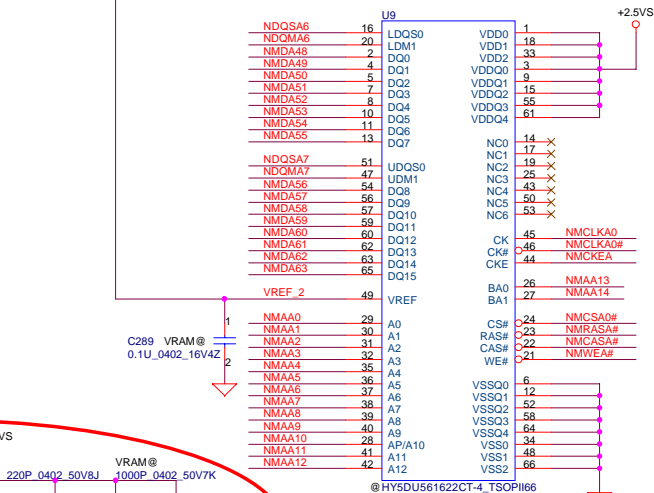
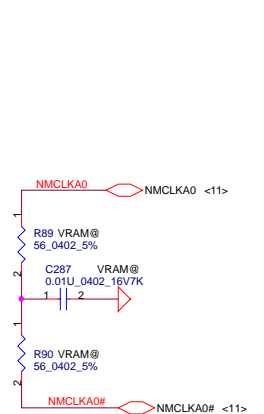
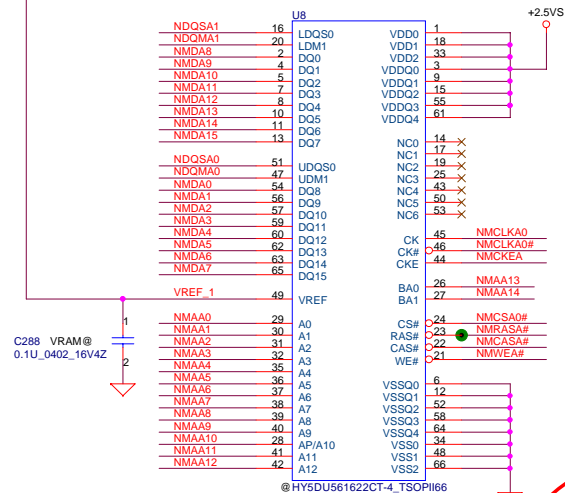
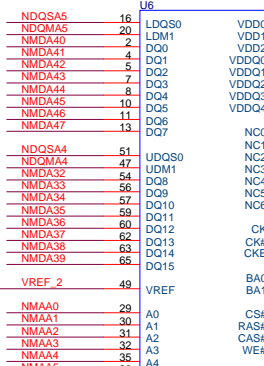
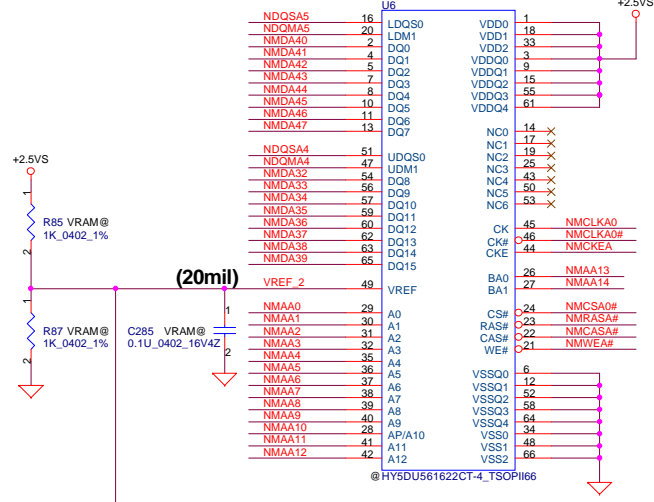
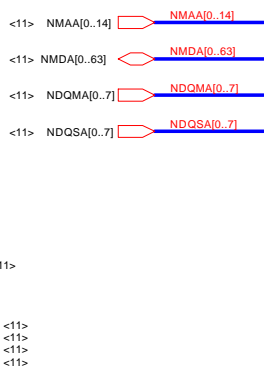
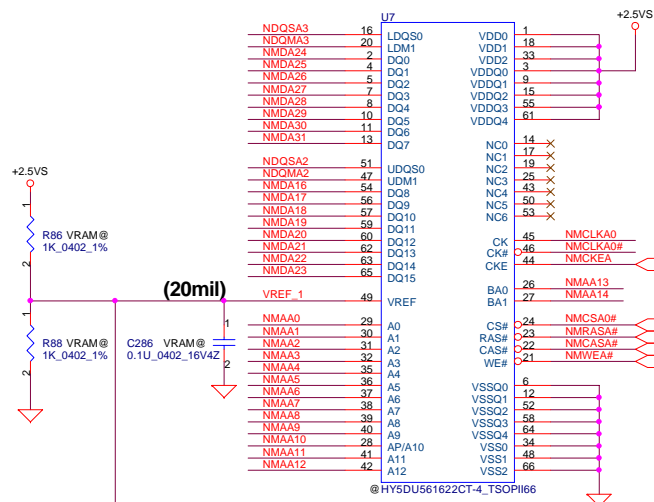
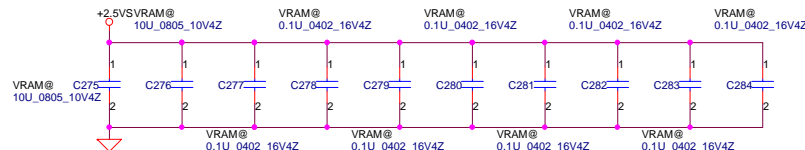
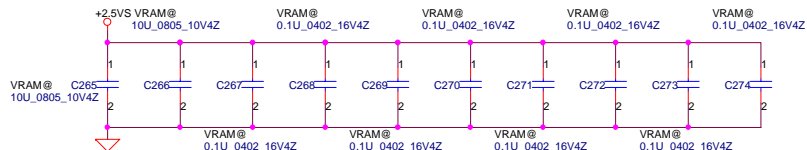
2005.08.11 for ATI Suggestion



2005.08.11 for ATI Suggestion

07/04 for +1.2V_HT ripple

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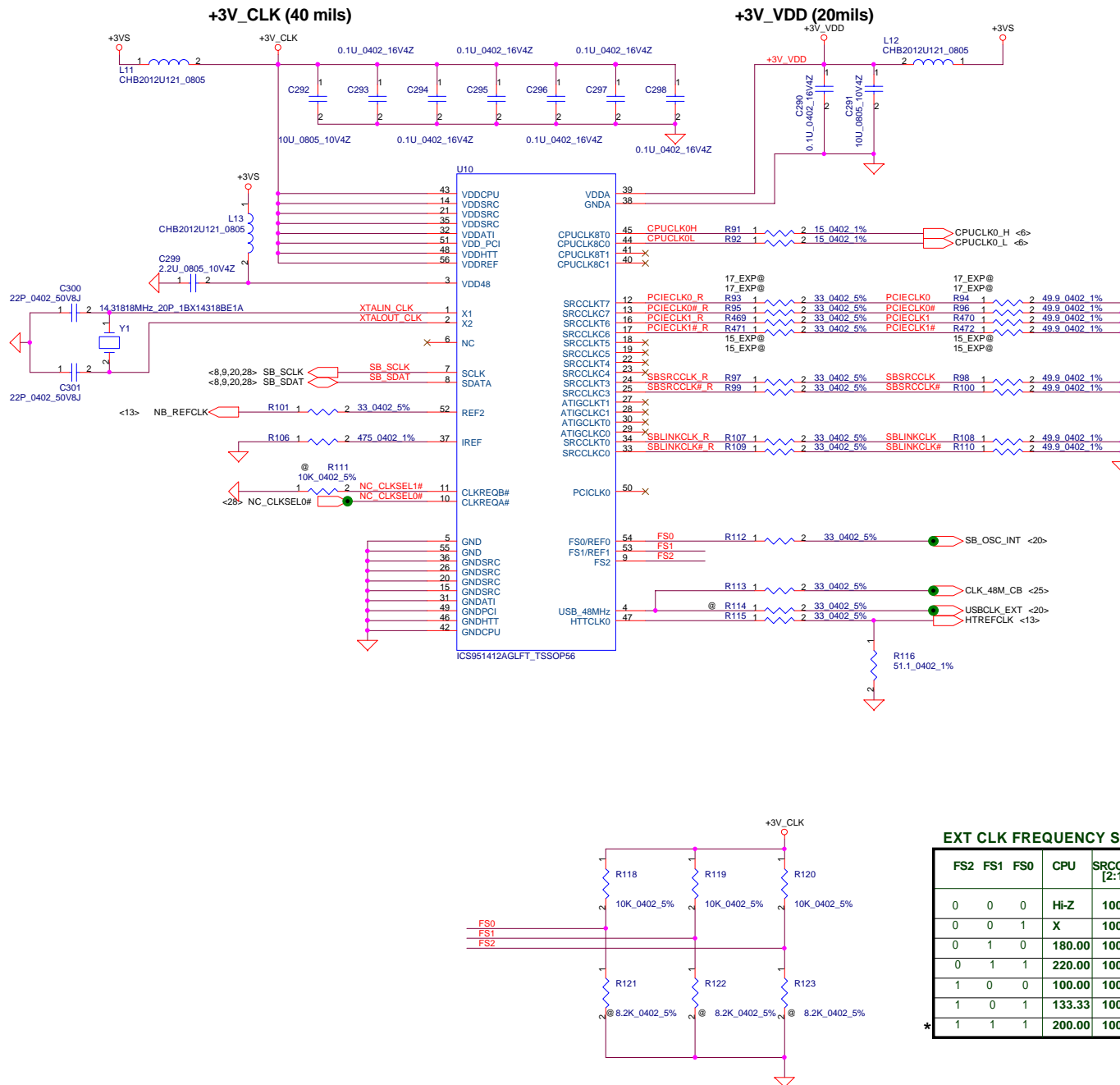


07/04 For EMI

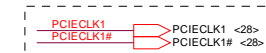
ZZZ
X76 VRAM
SAMSUNG® SAMSUNG X76 VRAM

ZZZ
X76 VRAM
HYNIX® HYNIX X76 VRAM

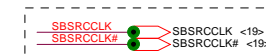
Security Classification		Compal Secret Data		Title	
Issued Date	2005/03/01	Deciphered Date	2005/04/06	VGA DDR	
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				Date Tuesday, August 30, 2005	Rev 0.8
				Sheet 15	of 53



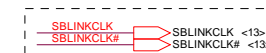
Express Card(17)



Express Card(15.4)



A link Express



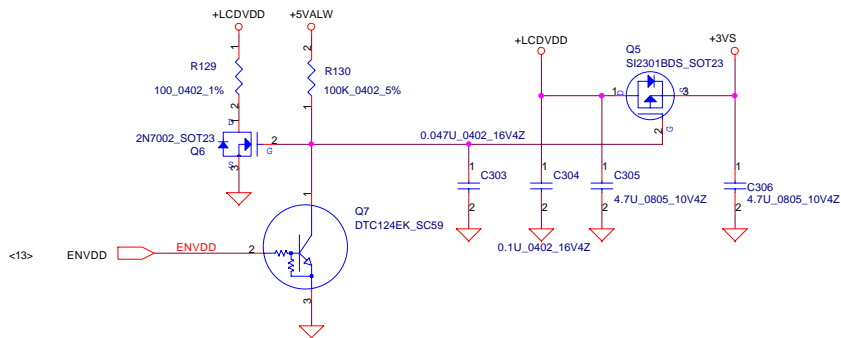
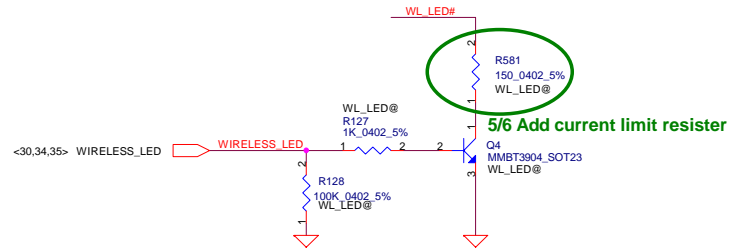
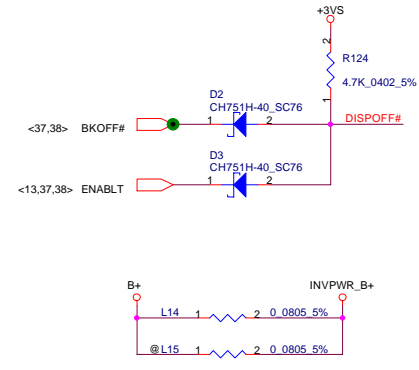
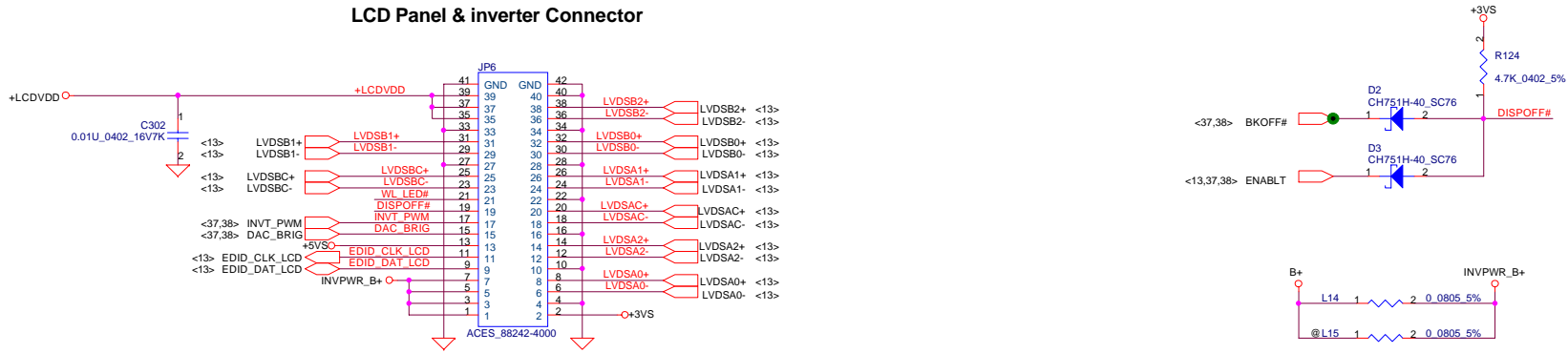
A link Express

EXT CLK FREQUENCY SELECT TABLE(MHZ)

FS2	FS1	FS0	CPU	SRCLK [2:1]	HTT	PCI	USB	COMMENT
0	0	0	Hi-Z	100.00	Hi-Z	Hi-Z	48.00	Reserved
0	0	1	X	100.00	X/3	X/6	48.00	Reserved
0	1	0	180.00	100.00	60.00	30.00	48.00	Reserved
0	1	1	220.00	100.00	36.56	73.12	48.00	Reserved
1	0	0	100.00	100.00	66.66	33.33	48.00	Reserved
1	0	1	133.33	100.00	66.66	33.33	48.00	Reserved
1	1	1	200.00	100.00	66.66	33.33	48.00	Normal HAMMER operation

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								Size Custom	Document Number			LA-2771		Rev
												0.8		
								Date:	Tuesday, August 30, 2005			Sheet	16	of

LCD Panel & inverter Connector

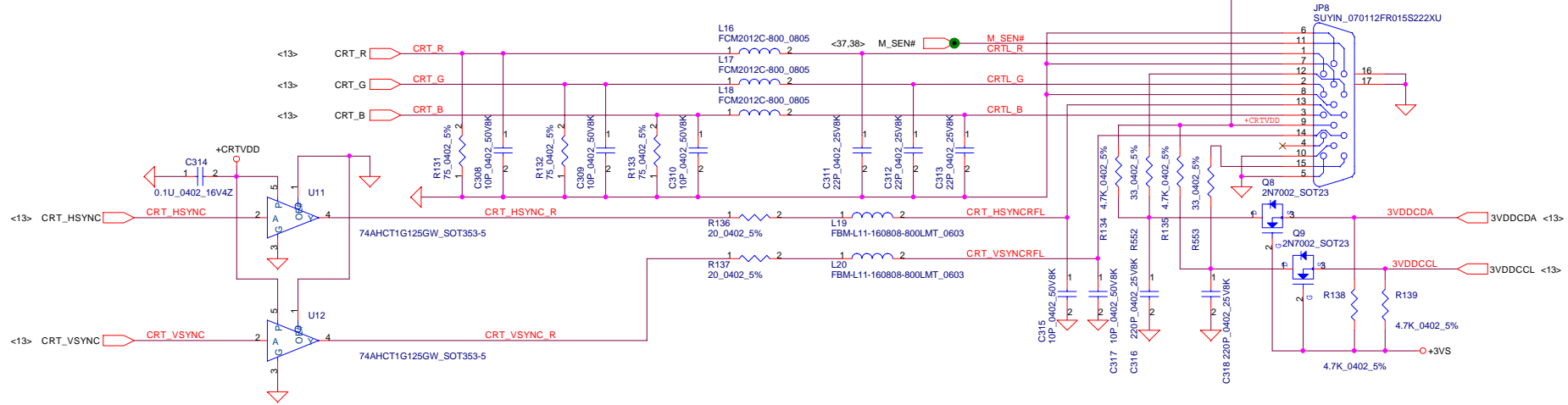


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				LA-2771				Tuesday, August 30, 2005			
				Sheet				17 of 53			

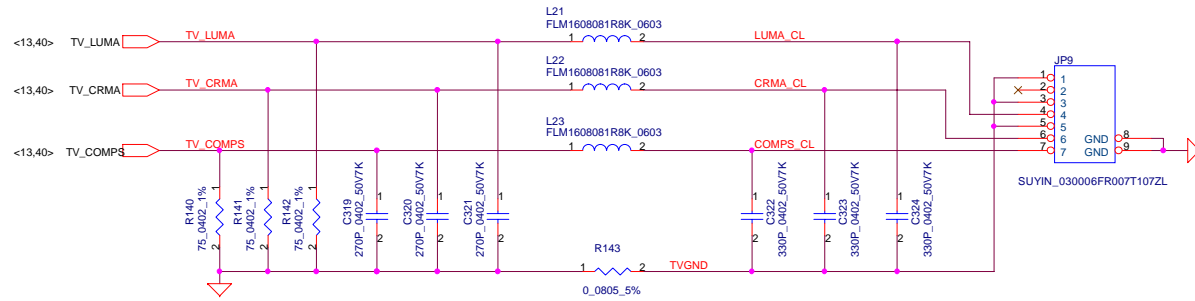
CRT CONNECTOR

+R_CRT_VCC , +CRTVDD (40mils)

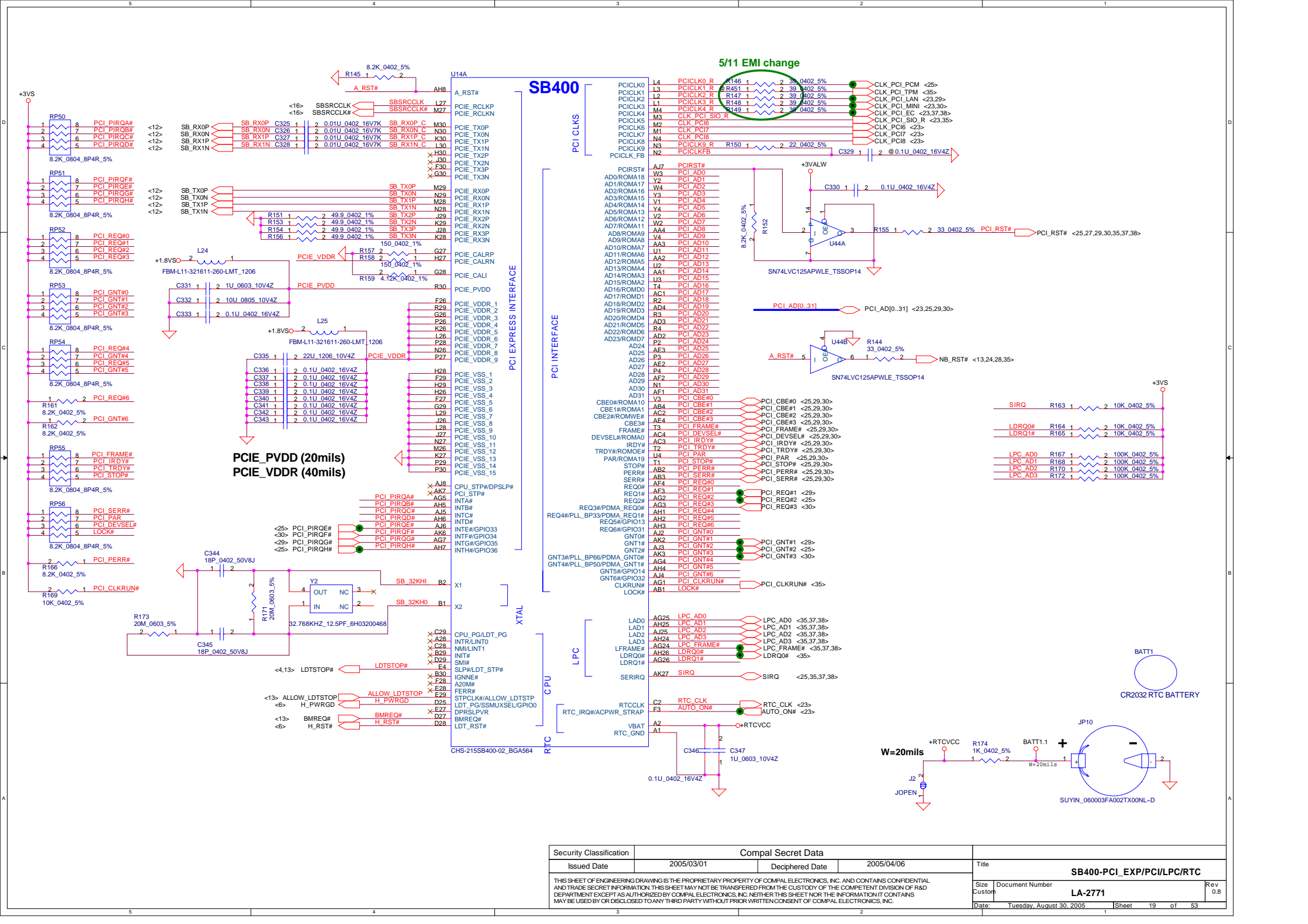
6/11 change D6 from RB411to RB491(higher current rating)

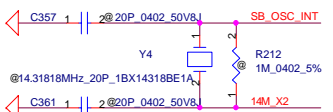
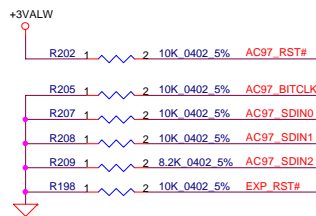
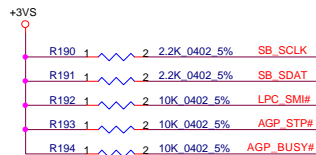
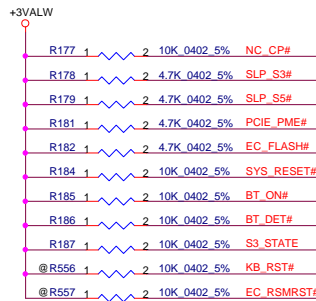


TV-Out Connector S-Video

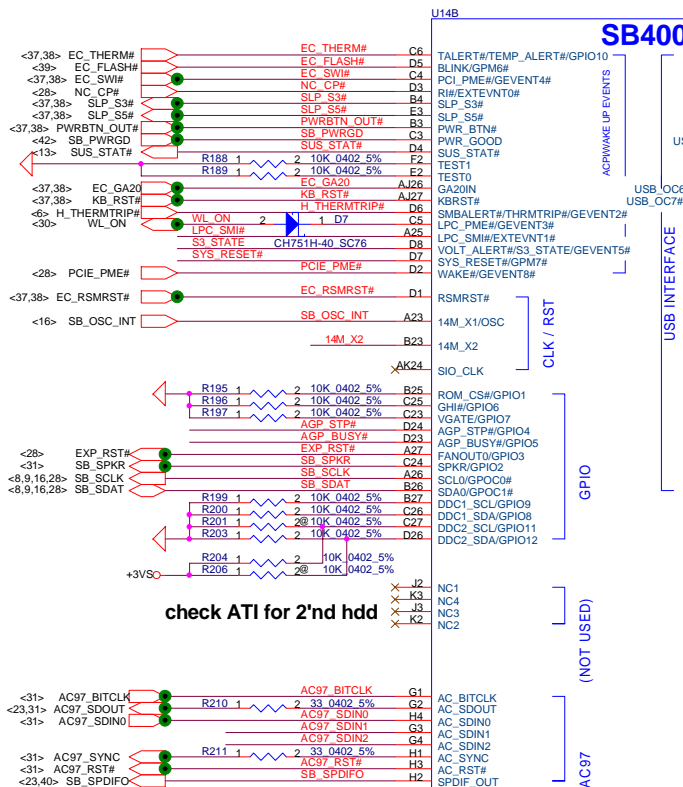


Security Classification				Compal Secret Data				Title			
Issued Date				2005/03/01				Deciphered Date			
								2005/04/06			
								CRT Connector & TV-OUT CONN			
								LA-2771			
								Rev 0.8			
								Date: Tuesday, August 30, 2005			
								Sheet 18 of 53			

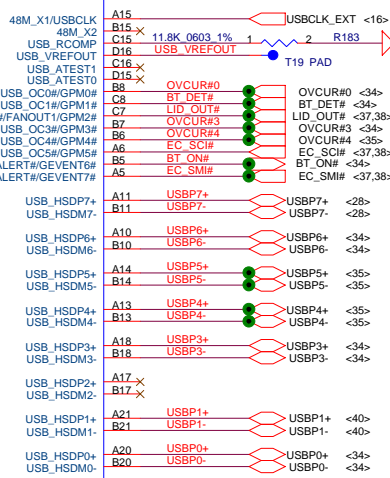




	GPI012	GPI011
* HYNIX 128MB	0	1
SAMSUNG 128MB	1	1
No VRAM	0	0
Reserved	1	0



CHS-215SB400-02_BGA564



Express Card 15.4

Bluetooth

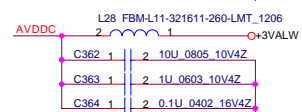
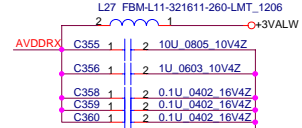
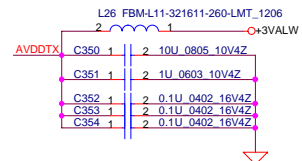
Right side USB

Right side USB

Left side USB

Docking

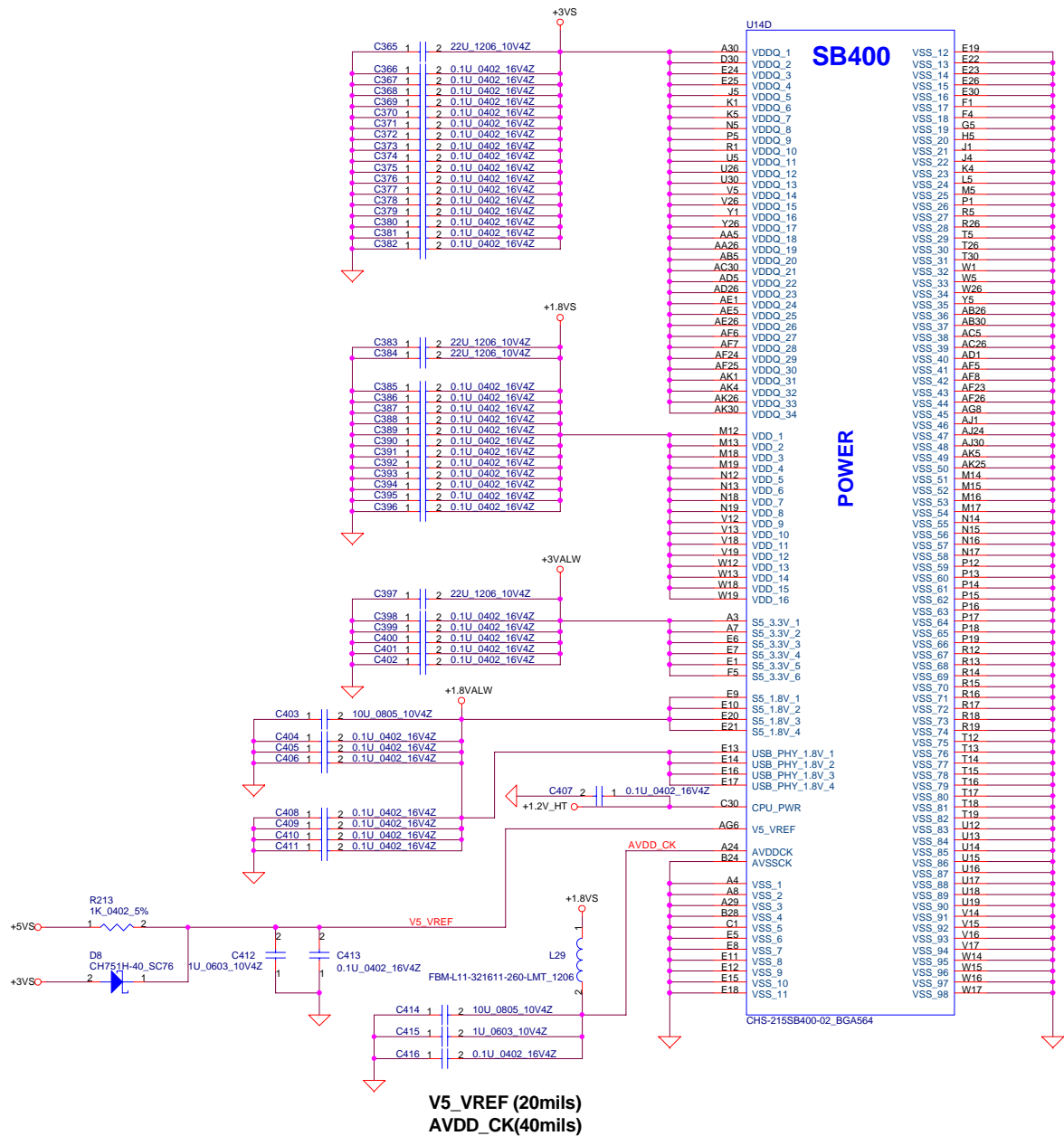
Left side USB



AVDDC (20mils)
AVDDTX, AVDDRDX (40mils)

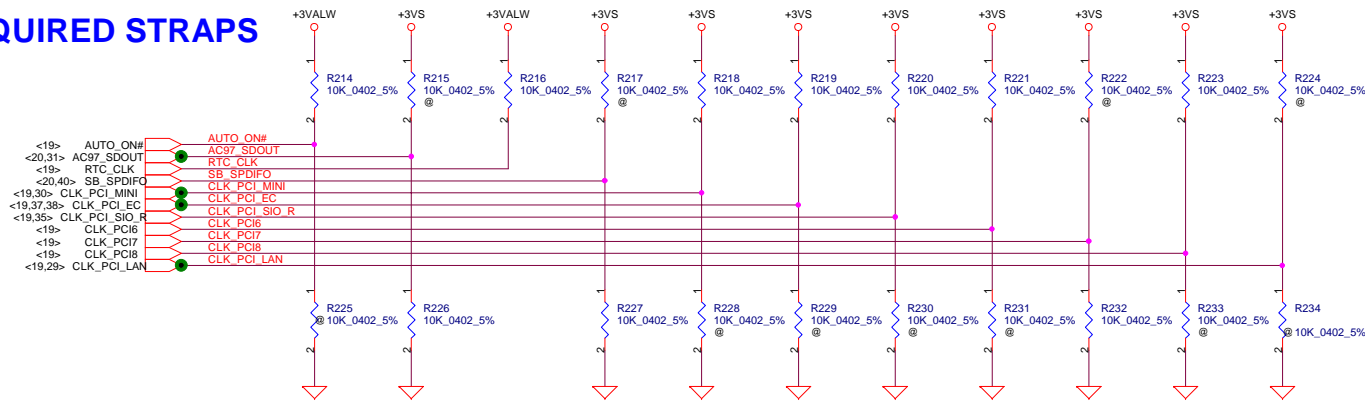
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Issued Date		2005/03/01		Deciphered Date		2005/04/06		Title					
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						Size		Document Number		LA-2771		Rev	
						Custom						0.8	
Date:						Tuesday, August 30, 2005		Sheet 20 of 53					

Security Classification	Compal Secret Data			Title		
Issued Date	2005/03/01	Deciphered Date	2005/04/06	SB400-IDE/SATA		
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Security Classification	Compal Secret Data			Title	
Issued Date	2005/03/01	Deciphered Date	2005/04/06	SB400-Power/GND	
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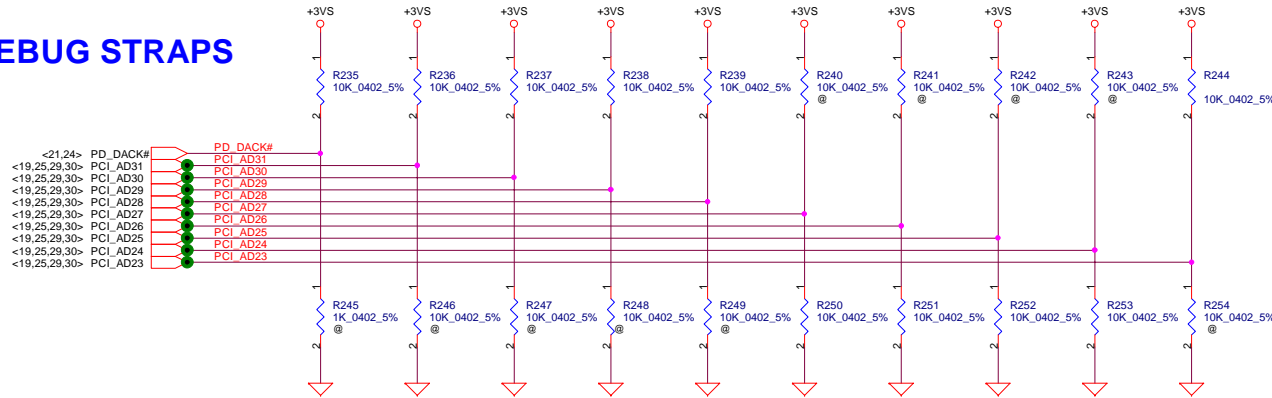
REQUIRED STRAPS



ACPWON

	AUTO_ON#	AC97_SDOOUT	RTC_CLK	SB_SPDIFO	CLK_PCI_LAN	CLK_PCI_MINI	CLK_PCI_EC	CLK_PCI_SIO	CLK_PCI6	CLK_PCI7	CLK_PCI8
PULL HIGH	MANUAL PWR ON DEFAULT	USE DEBUG STRAPS	INTERNAL RTC DEFAULT	SIO 24MHz	48MHz OSC MODE	USB PHY PWRDOWN DISABLE DEFAULT	INTERNAL 48MHz DEFAULT	PCIE_CM_SET LOW DEFAULT	CPU I/F = K8 DEFAULT	ROM TYPE H,H = PCI ROM H,L = PMC LPC ROM	
PULL LOW	AUTO PWR ON	IGNORE DEBUG STRAPS DEFAULT	EXTERNAL RTC (NOT SUPPORTED W/ IT8712)	SIO 48MHz DEFAULT	48MHz XTAL MODE	USB PHY PWRDOWN ENABLE	EXTERNAL 48MHz	PCIE_CM_SET High	CPU I/F = P4	L,H = NORMAL LPC ROM L,L = FWH ROM DEFAULT	

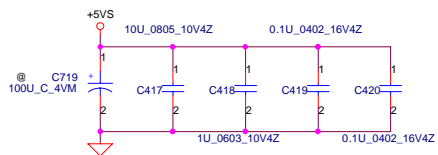
DEBUG STRAPS



	PD_DACK#	PCI_AD31	PCI_AD30	PCI_AD29	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	RESERVED	RESERVED	RESERVED	RESERVED	BYPASS PCI PLL	BYPASS ACPI BCLK DEFAULT	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	RESERVED
PULL LOW	USE SHORT RESET					USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	

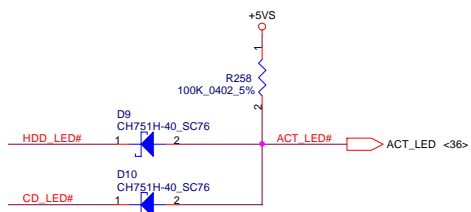
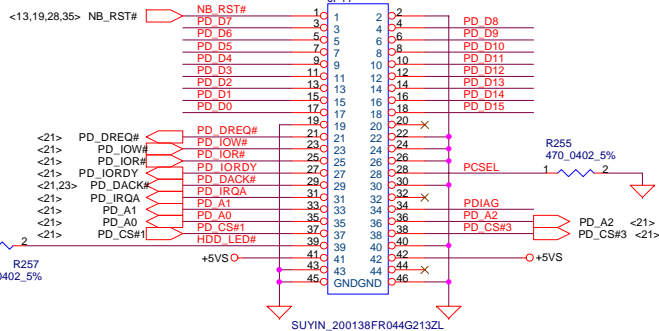
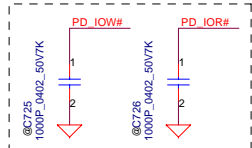
Security Classification	Compal Secret Data			Title	
Issued Date	2005/03/01	Deciphered Date	2005/04/06	Hardware Trap	
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Main HDD

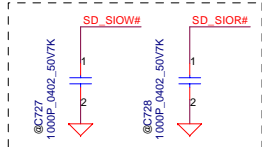


<21> PD_D[0..15] PD_DI[0..15]

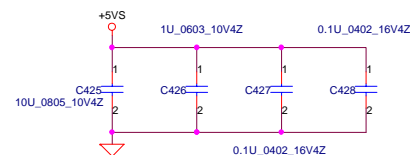
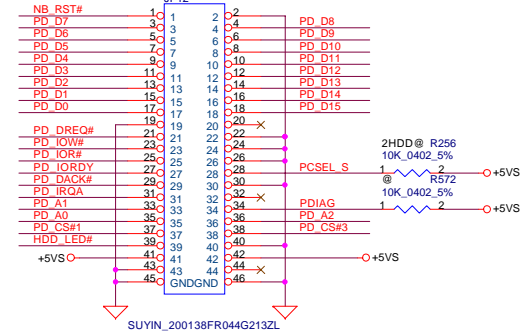
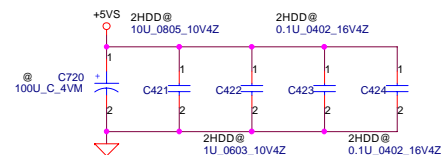
EMI



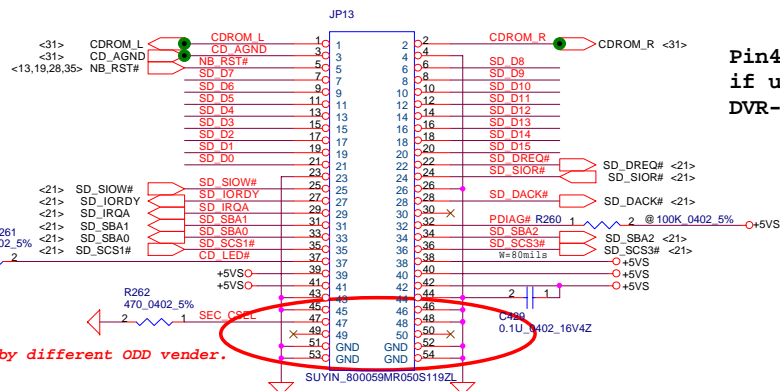
EMI



Second HDD



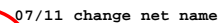
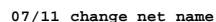
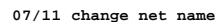
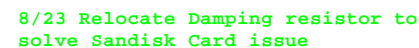
<21> SD_D[0..15] SD_DI[0..15]



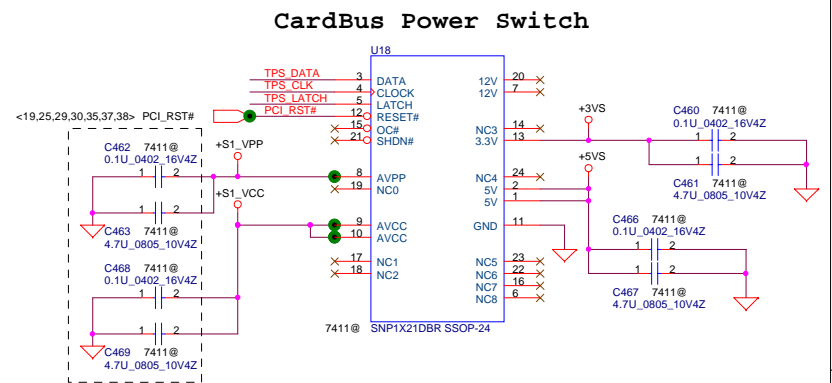
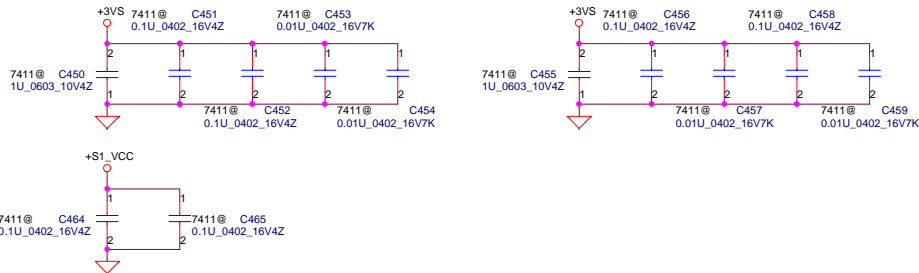
07/11 for defined by different ODD vender.

Pin4 of CD_ROM connector is NC
if use Pioneer ODD(DVD Dual
DVR-K12TBC/DVR-K13TBC)

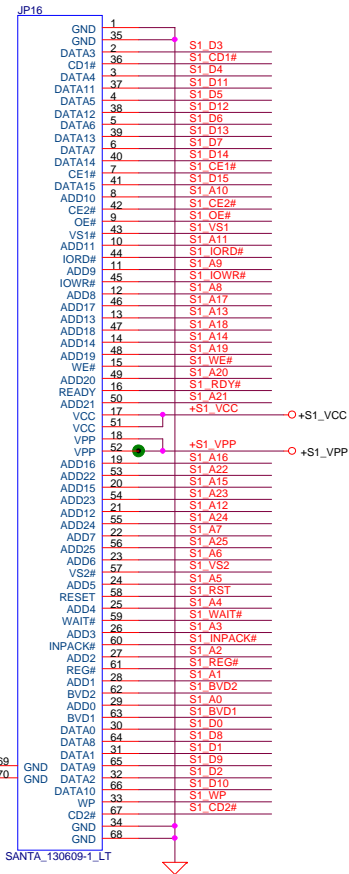
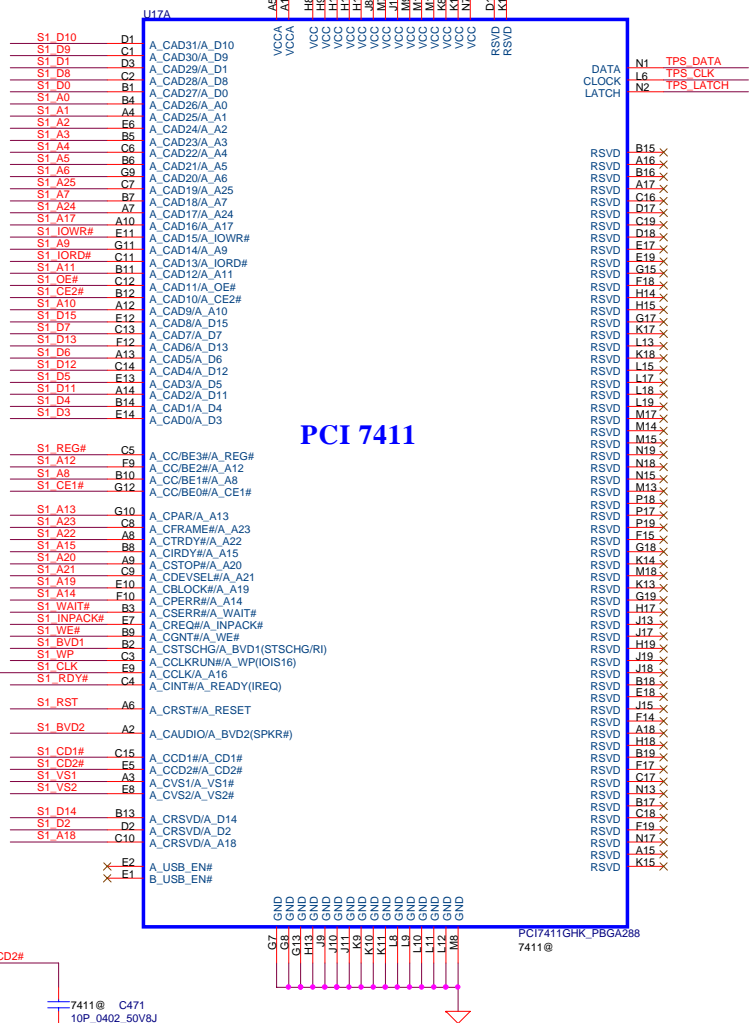
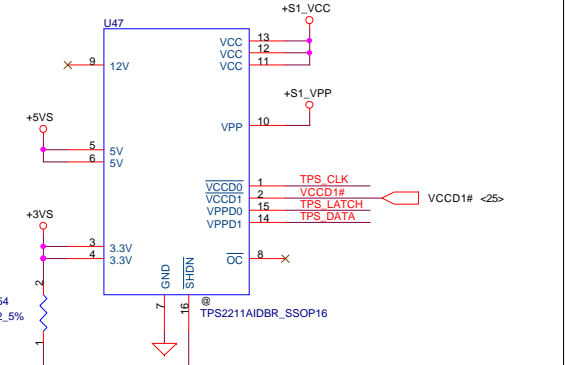
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Issued Date	2005/03/01	Deciphered Date	2005/04/06	HDD/CDROM		
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								Custom	LA-2771			0.8	
								Date:	Tuesday, August 30, 2005		Sheet	26	of

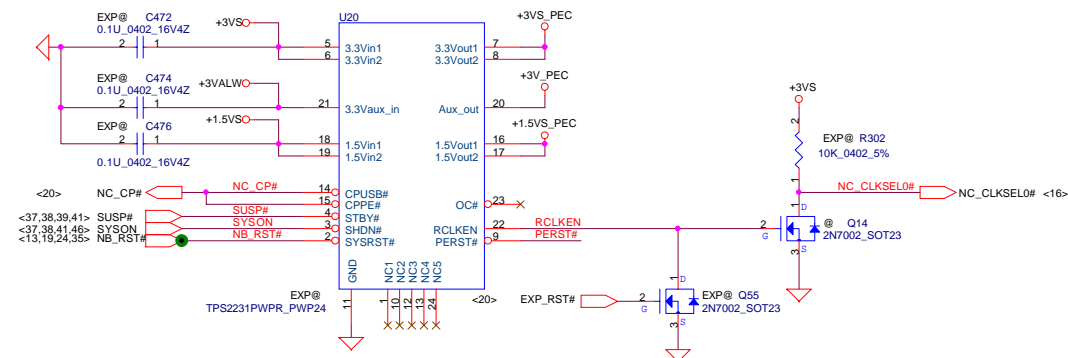


close to card bus conn

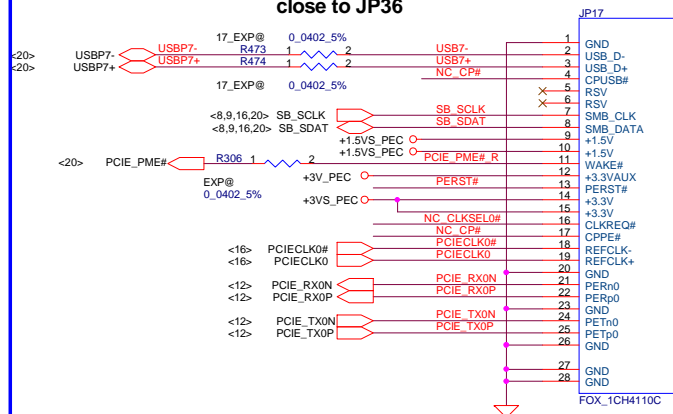


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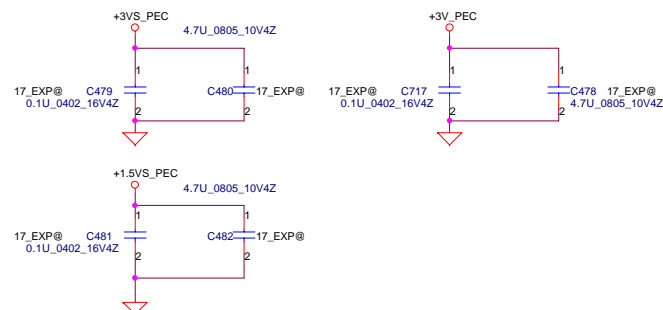
Express Card Power Switch



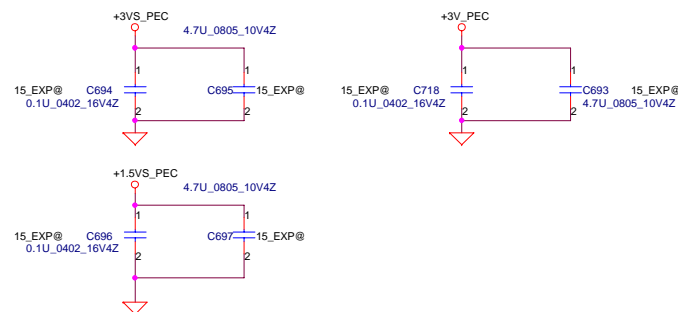
close to JP36



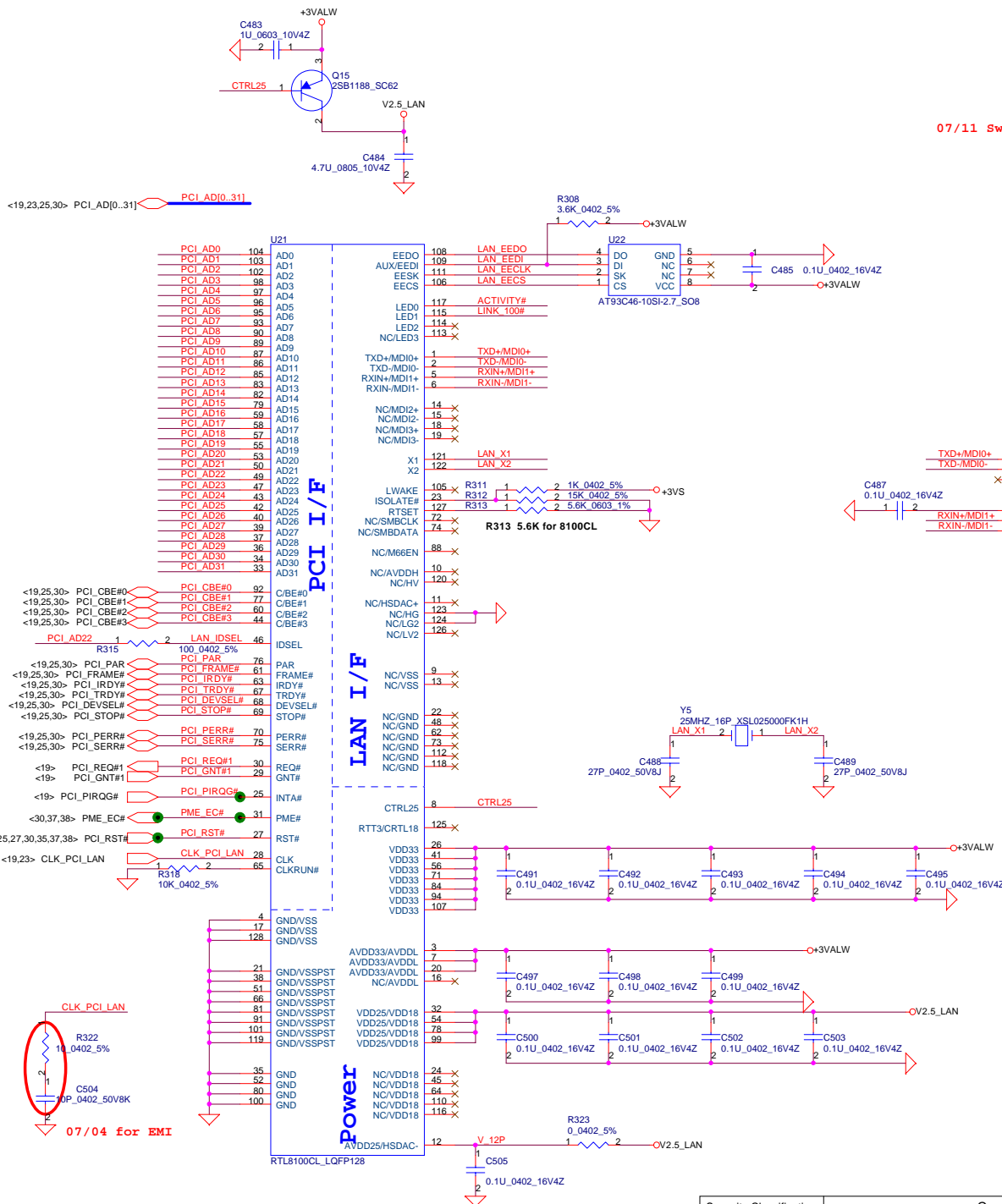
Near to Express Card slot. 17



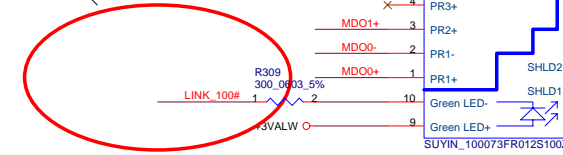
Near to Express Card slot. 15.4



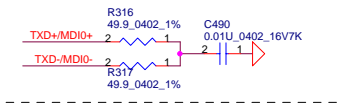
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Issued Date	2005/03/01	Deciphered Date	2005/04/06	Express Card	
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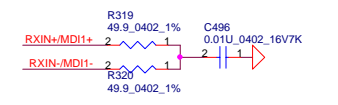
07/11 Swap net for HP request



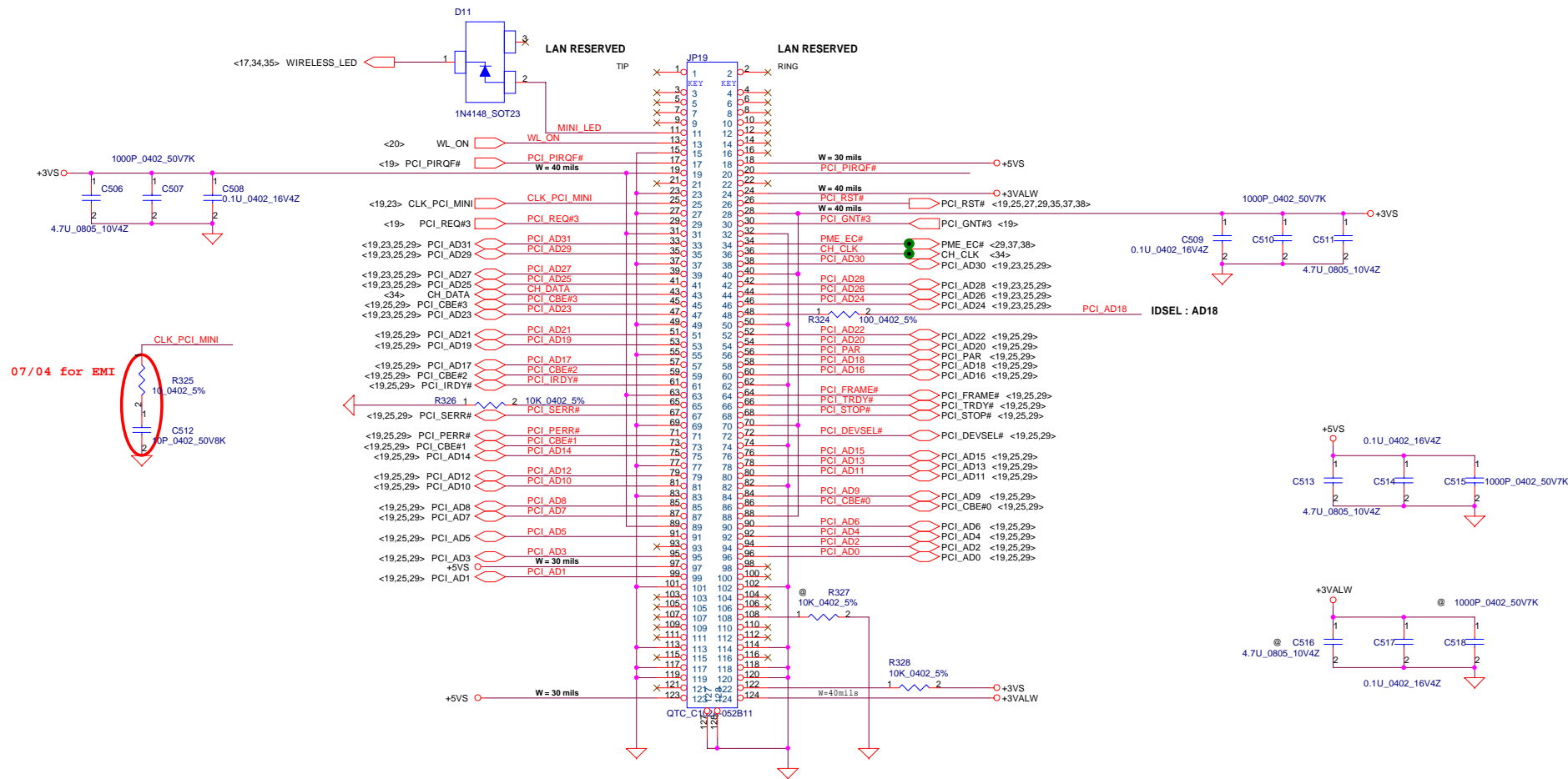
close to chip



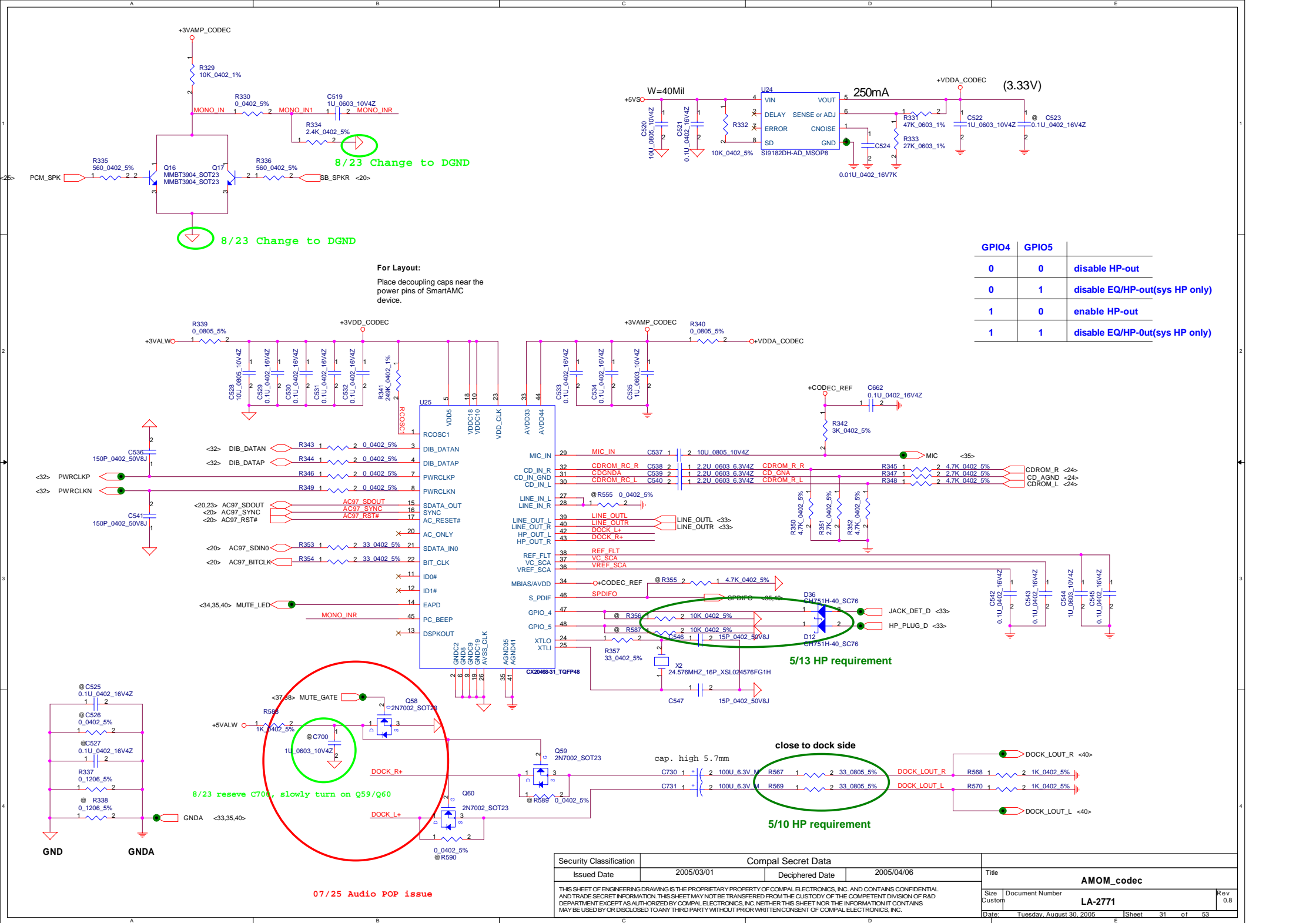
close to magnetic

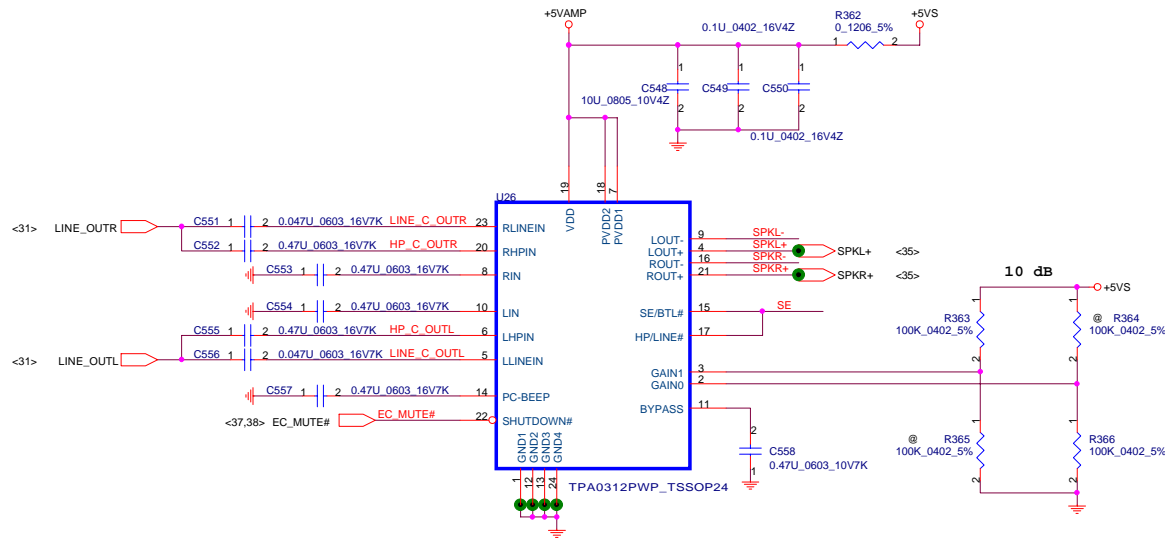


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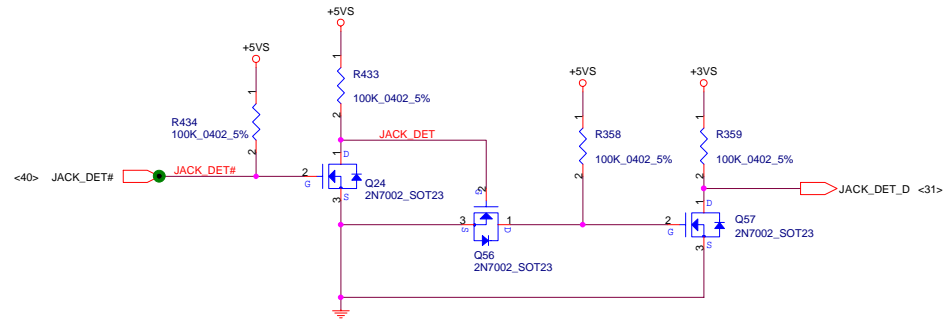
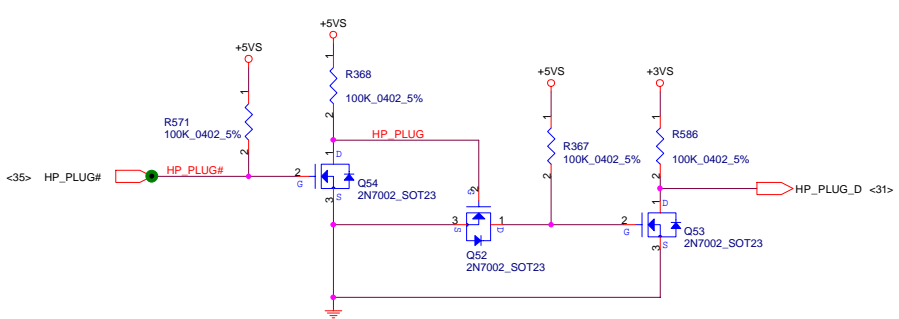
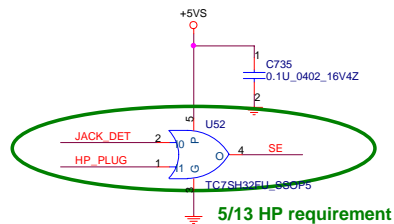
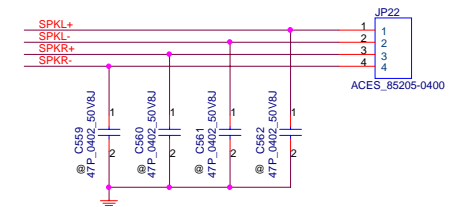


Security Classification		Compal Secret Data		Title	
Issued Date	2005/03/01	Deciphered Date	2005/04/06	Mini PCI	
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Gain Settings			
GAIN0	GAIN1	SE/BTL#	Av(inv)
0	0	0	6 dB
0	1	0	* 10 dB
1	0	0	15.6 dB
1	1	0	21.6 dB
X	X	1	4.1 dB



Security Classification				Compal Secret Data				Title			
Issued Date				Deciphered Date				AMP & Audio jack			
2005/03/01				2005/04/06				LA-2771			
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Custom				Document Number				0.8			
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Security Classification	Compal Secret Data					
Issued Date	2005/03/01	Deciphered Date	2005/04/06	Title		
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				Size	Document Number	Rev
					LA-2771	0
				Date	Tuesday, August 30, 2005	Sheet 34 of 53

INT_KBD CONN.(TYPE "D" KB)

KSIO0_71 KSIO[0..7] <34,37,38>
KSO0[0..17] KSO[0..17] <34,37,38>

JP27
KS17 26
KS10 25
KS15 24
KS11 23
KS14 22
KS16 21
KS13 20
KS12 19
KS01 18
KS02 17
KS04 16
KS00 15
KS016 14
KS05 13
KS06 12
KS03 11
KS07 10
KS08 9
KS09 8
KS010 7
KS011 6
KS012 5
KS013 4
KS014 3
KS015 2
KS017 1

ACES_85201-2605

KS17 C583 D@ 1 2 100P_0402_50V8J
KS10 C584 D@ 1 2 100P_0402_50V8J
KS15 C585 D@ 1 2 100P_0402_50V8J
KS11 C586 D@ 1 2 100P_0402_50V8J
KS14 C587 D@ 1 2 100P_0402_50V8J
KS16 C588 D@ 1 2 100P_0402_50V8J
KS13 C589 D@ 1 2 100P_0402_50V8J
KS12 C590 D@ 1 2 100P_0402_50V8J
KSO1 C591 D@ 1 2 100P_0402_50V8J
KSO2 C592 D@ 1 2 100P_0402_50V8J
KSO4 C593 D@ 1 2 100P_0402_50V8J
KSO0 C594 D@ 1 2 100P_0402_50V8J
KSO16 C596 D@ 1 2 100P_0402_50V8J
KSO5 C597 D@ 1 2 100P_0402_50V8J
KSO6 C598 D@ 1 2 100P_0402_50V8J
KSO3 C599 D@ 1 2 100P_0402_50V8J
KSO7 C600 D@ 1 2 100P_0402_50V8J
KSO8 C601 D@ 1 2 100P_0402_50V8J
KSO9 C602 D@ 1 2 100P_0402_50V8J
KSO10 C603 D@ 1 2 100P_0402_50V8J
KSO11 C604 D@ 1 2 100P_0402_50V8J
KSO12 C605 D@ 1 2 100P_0402_50V8J
KSO13 C606 D@ 1 2 100P_0402_50V8J
KSO14 C607 D@ 1 2 100P_0402_50V8J
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KSO17 C661 D@ 1 2 100P_0402_50V8J

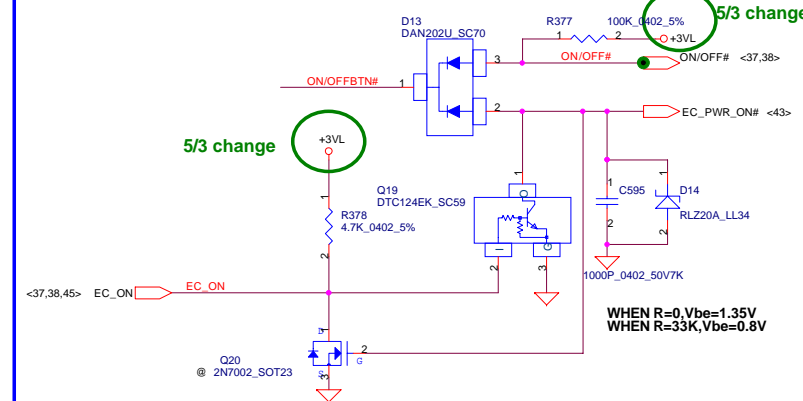
KS11 C663 C@ 1 2 100P_0402_50V8J
KS17 C664 C@ 1 2 100P_0402_50V8J
KS16 C665 C@ 1 2 100P_0402_50V8J
KSO9 C666 C@ 1 2 100P_0402_50V8J
KS14 C667 C@ 1 2 100P_0402_50V8J
KS15 C668 C@ 1 2 100P_0402_50V8J
KSO0 C669 C@ 1 2 100P_0402_50V8J
KS12 C670 C@ 1 2 100P_0402_50V8J
KS13 C671 C@ 1 2 100P_0402_50V8J
KSO5 C672 C@ 1 2 100P_0402_50V8J
KSO1 C673 C@ 1 2 100P_0402_50V8J
KSO0 C674 C@ 1 2 100P_0402_50V8J
KSO2 C675 C@ 1 2 100P_0402_50V8J
KSO4 C676 C@ 1 2 100P_0402_50V8J
KSO7 C677 C@ 1 2 100P_0402_50V8J
KSO8 C678 C@ 1 2 100P_0402_50V8J
KSO6 C679 C@ 1 2 100P_0402_50V8J
KSO3 C680 C@ 1 2 100P_0402_50V8J
KSO12 C681 C@ 1 2 100P_0402_50V8J
KSO10 C682 C@ 1 2 100P_0402_50V8J
KSO14 C683 C@ 1 2 100P_0402_50V8J
KSO11 C684 C@ 1 2 100P_0402_50V8J
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KSO15 C686 C@ 1 2 100P_0402_50V8J

15.4 (TYPE "C" KB)

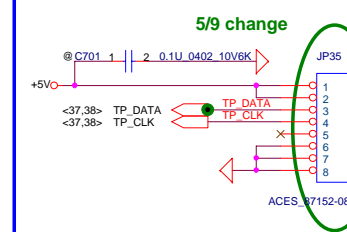
JP20
KS11 24
KS17 23
KS16 22
KSO9 21
KS14 20
KSO0 19
KS12 18
KS01 17
KS13 16
KS05 15
KS07 14
KS02 13
KS04 12
KS03 11
KS06 10
KS08 9
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KS012 7
KS014 6
KS011 5
KS010 4
KS015 3
KS010 2
KS015 1

ACES_85201-2405

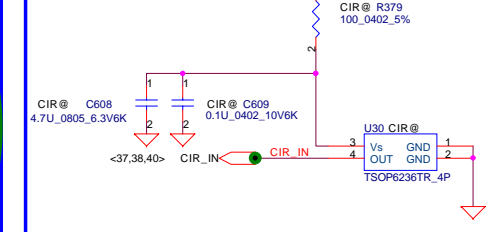
Power BTN



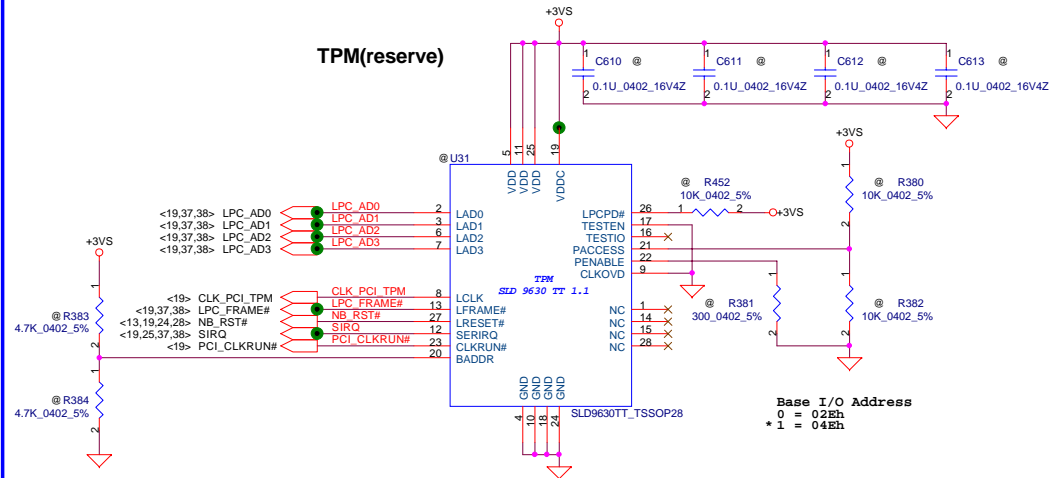
TP to MB CONN



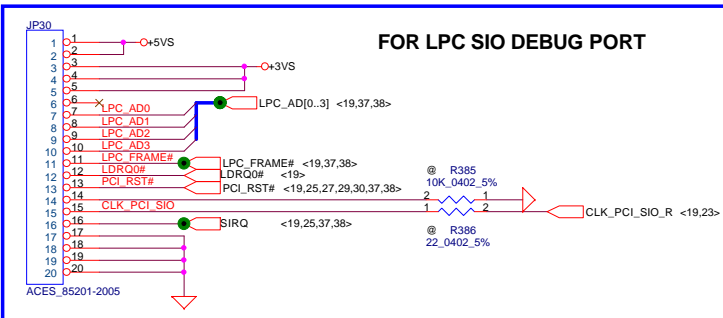
Consumer IR



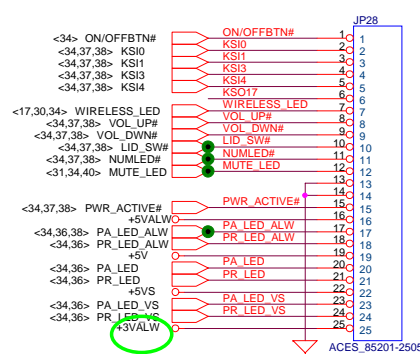
TPM(reserve)



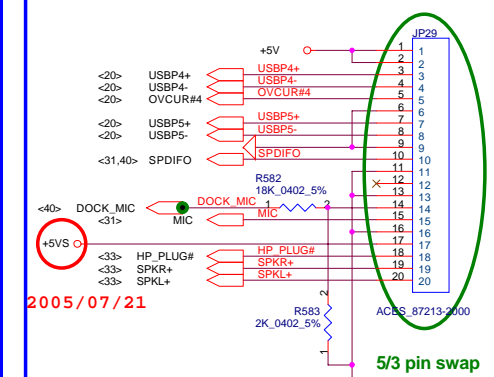
FOR LPC SIO DEBUG PORT



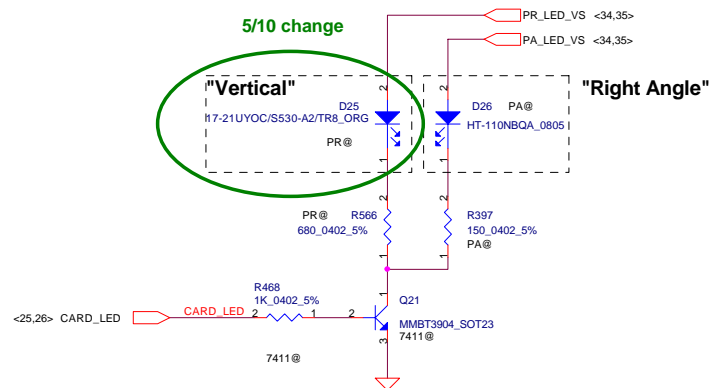
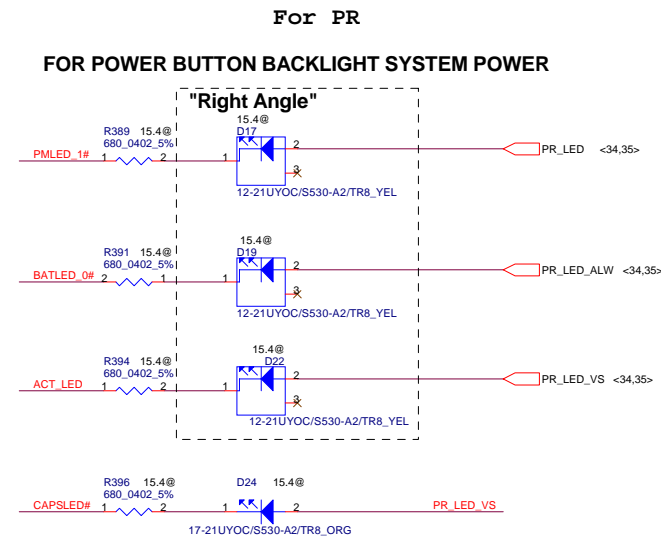
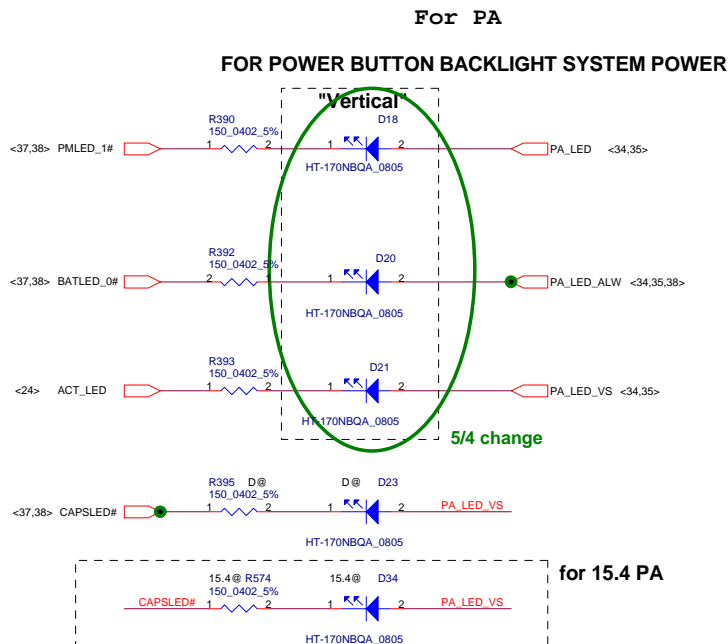
Switch board conn



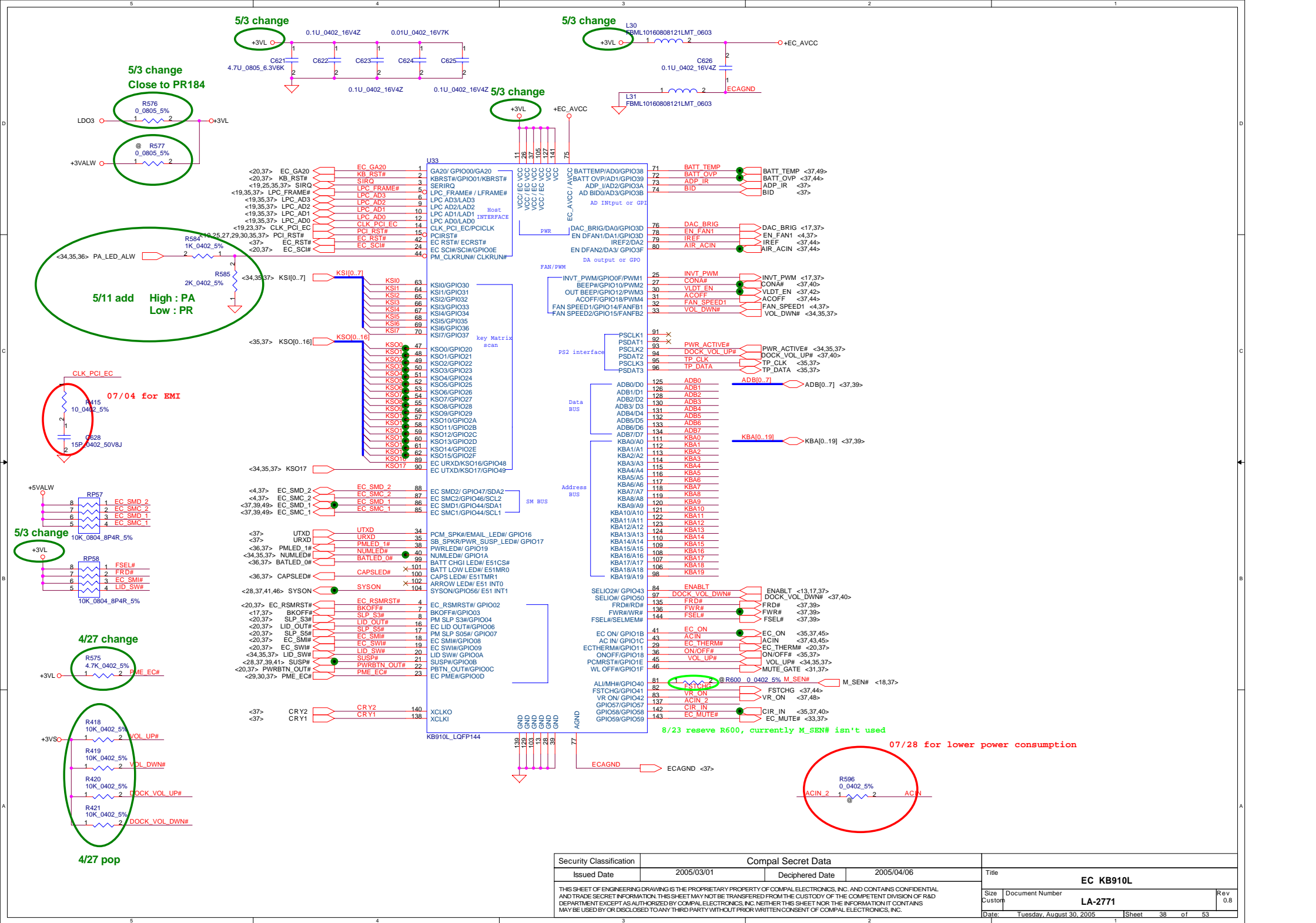
Audio board conn



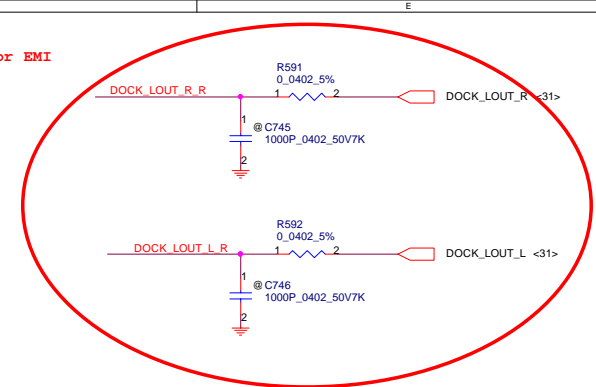
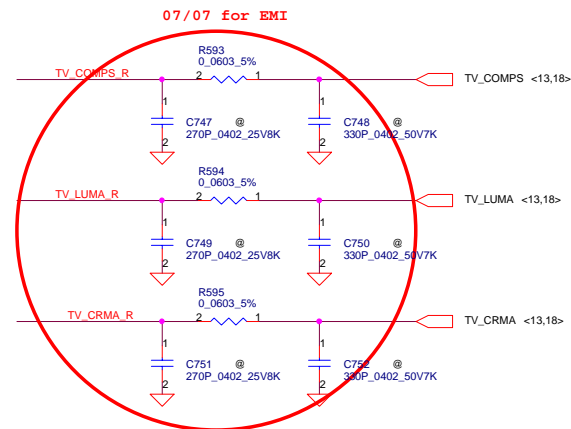
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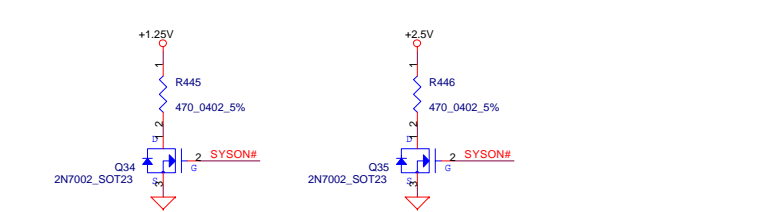
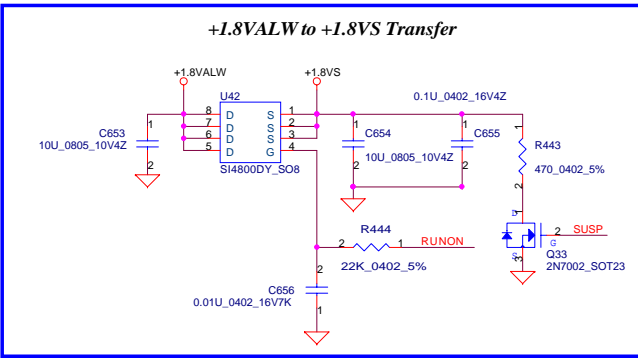
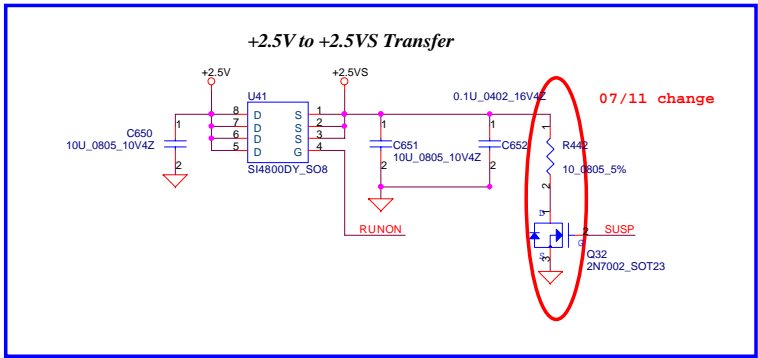
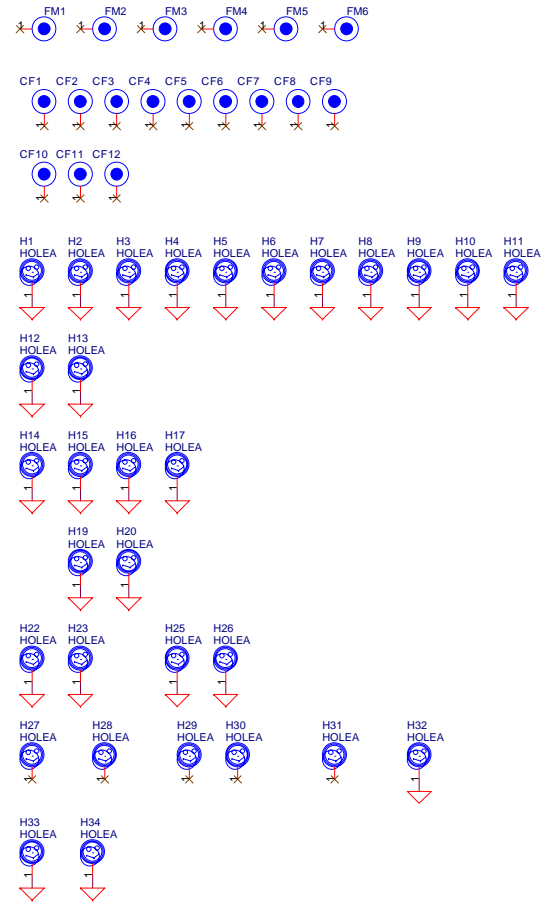
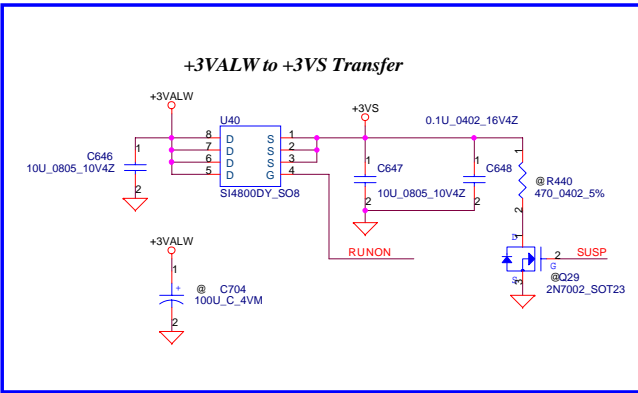
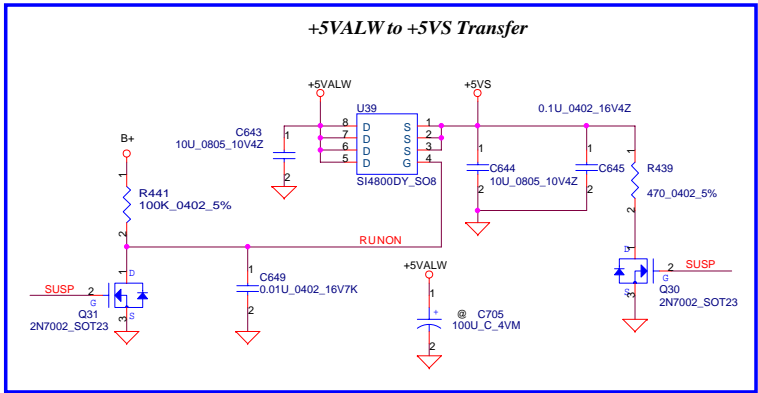
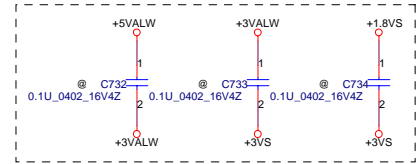
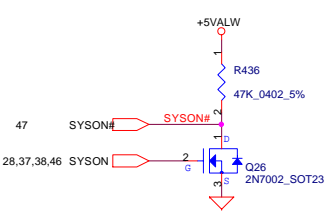
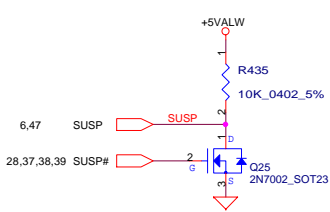
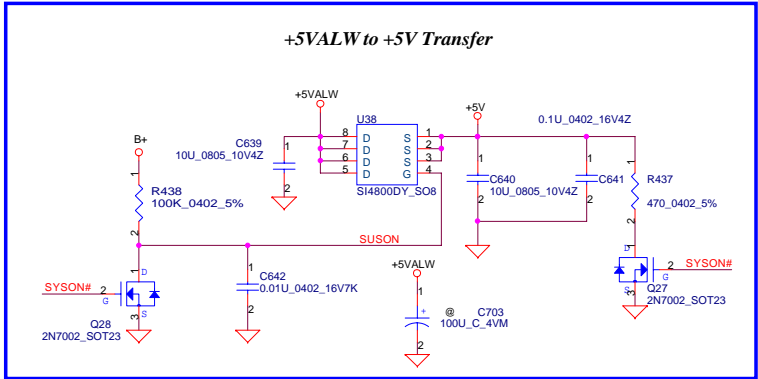
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Issued Date	2005/03/01	Deciphered Date	2005/04/06	INDICATE LED		
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				Custom	LA-2771	0.8
				Date	Tuesday, August 30, 2005	Sheet 36 of 53



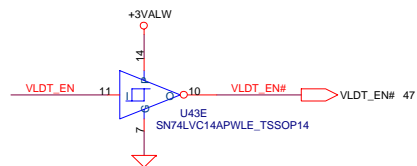
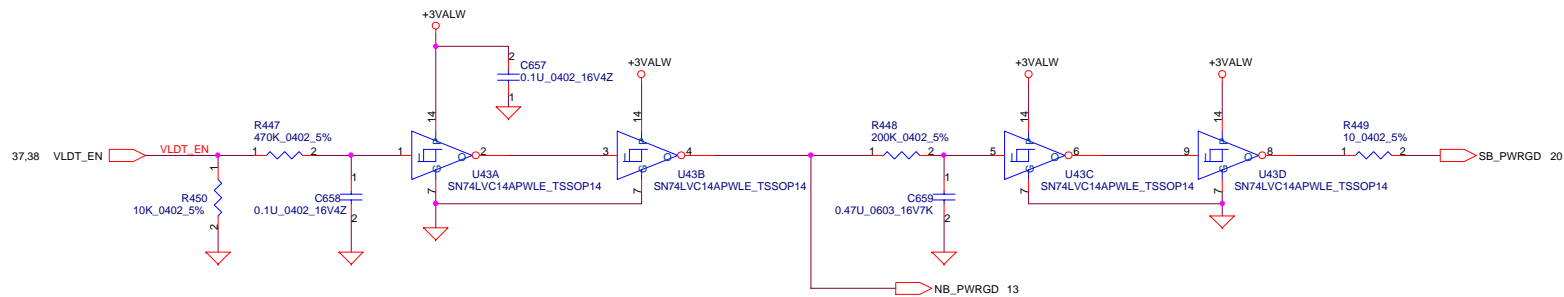
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				Size Custom	Document Number LA-2771	Rev 0.8
				Date:	Tuesday, August 30, 2005	Sheet 39 of 53

[illegible]

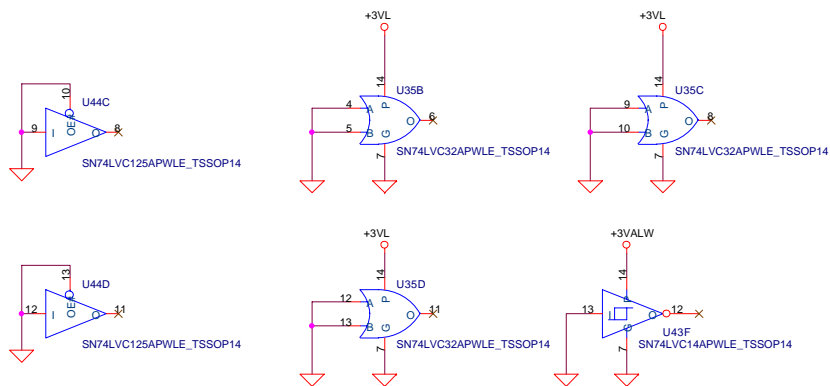
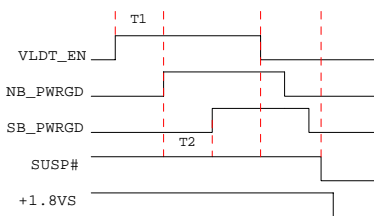
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Issued Date	2005/03/01	Deciphered Date	2005/04/06	Title	DOCK CONN		
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Issued Date	2005/03/01	Deciphered Date	2005/04/06			
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					Date:	Tuesday, August 30, 2005
					Sheet	41 of 53

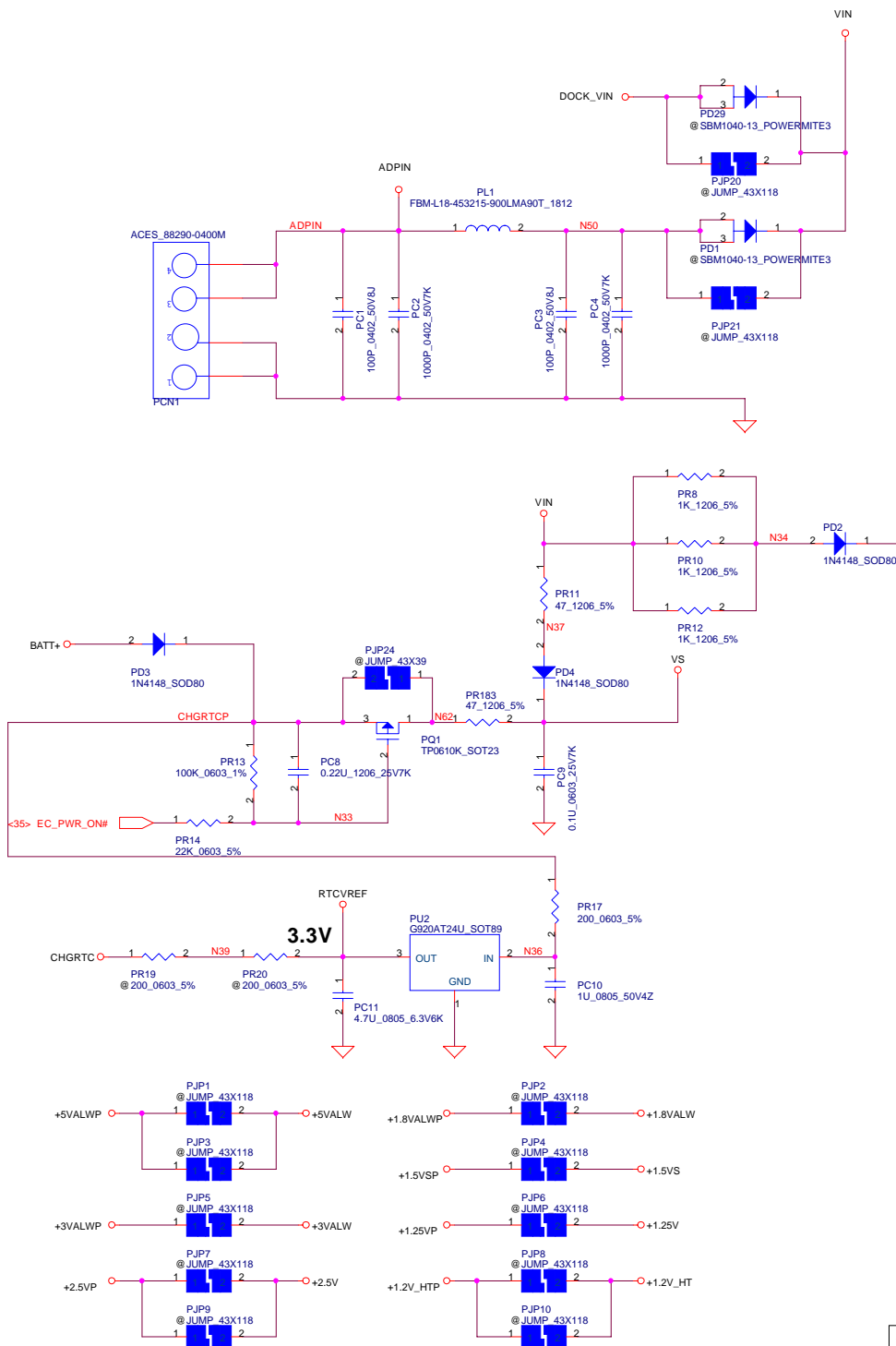


note:T1 minimum 15ms,T2 minimum 33ms/maximum 500ms,
SUSP# goes to low after SB_PWRGD goes to low for power
down.



Security Classification		Compal Secret Data		Title	
Issued Date	2005/03/01	Deciphered Date	2005/04/06	P_OK	
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				Custom	LA-2771
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				Rev	0.8

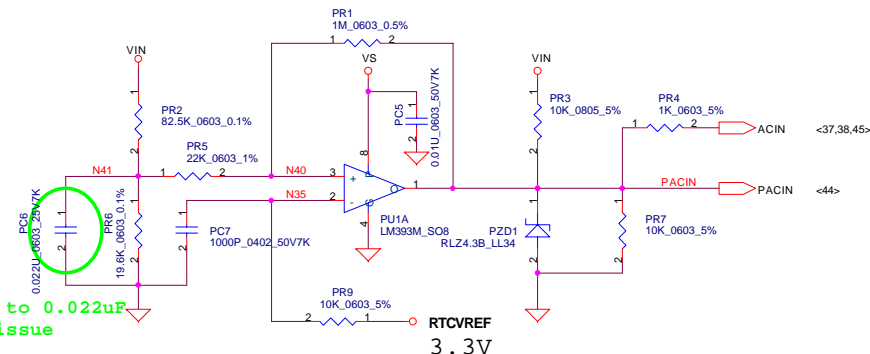
Detector



Vin Detector : Cayenne

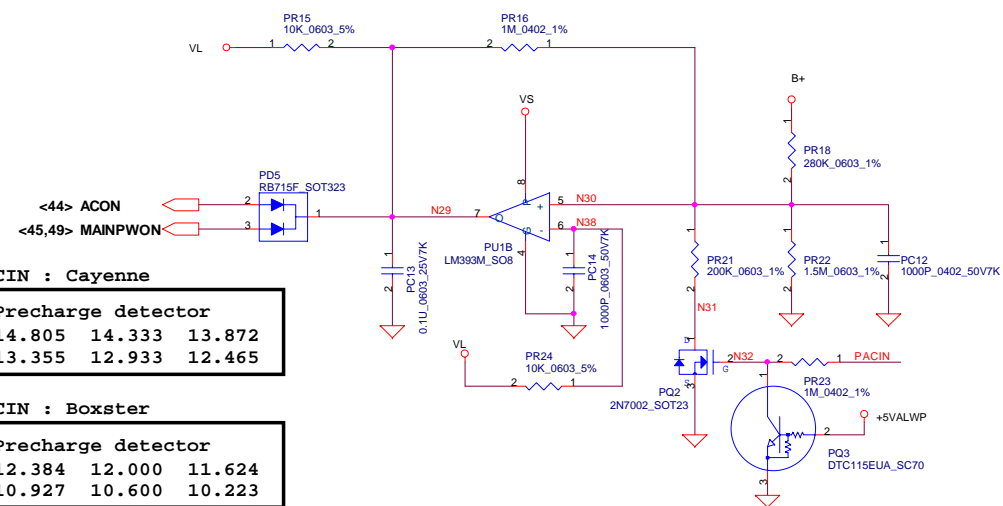
18.234	17.841	17.449
17.597	17.210	16.813

Vin Detector : Boxster		
14.352	13.950	13.555
13.818	13.411	13.000



8/29 Change to 0
for AC Off issue

Cayenne : PR5=22K; PR6=19.6K
Boxster : PR5=47K; PR6=27K



ACIN : Cayenne

Precharge detector		
14.805	14.333	13.872
13.355	12.933	12.465

ACIN : Boxster

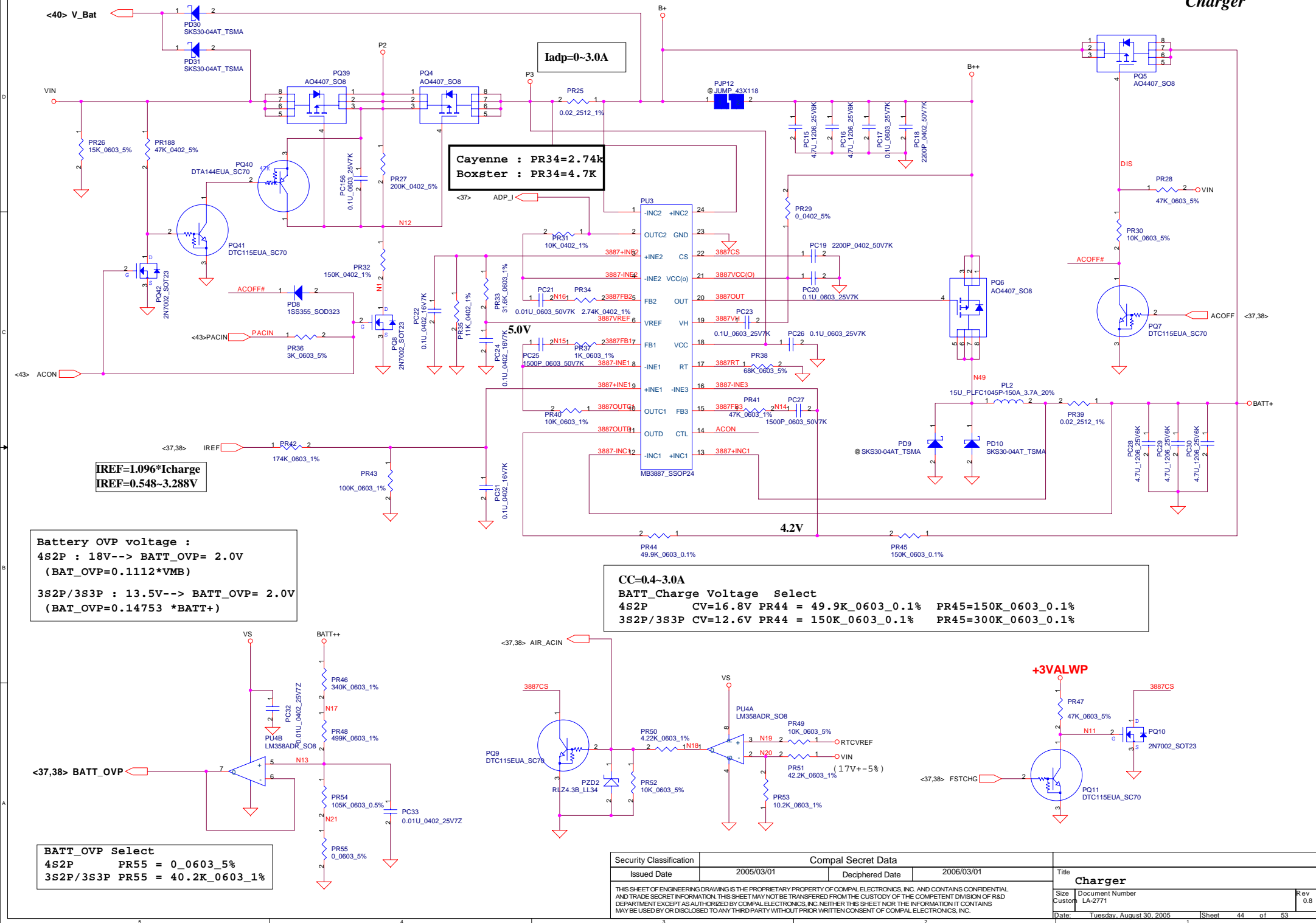
Precharge detector		
12.384	12.000	11.624
10.927	10.600	10.223

BATT		
Detector		
7.558	7.333	7.112
6.108	5.933	5.704

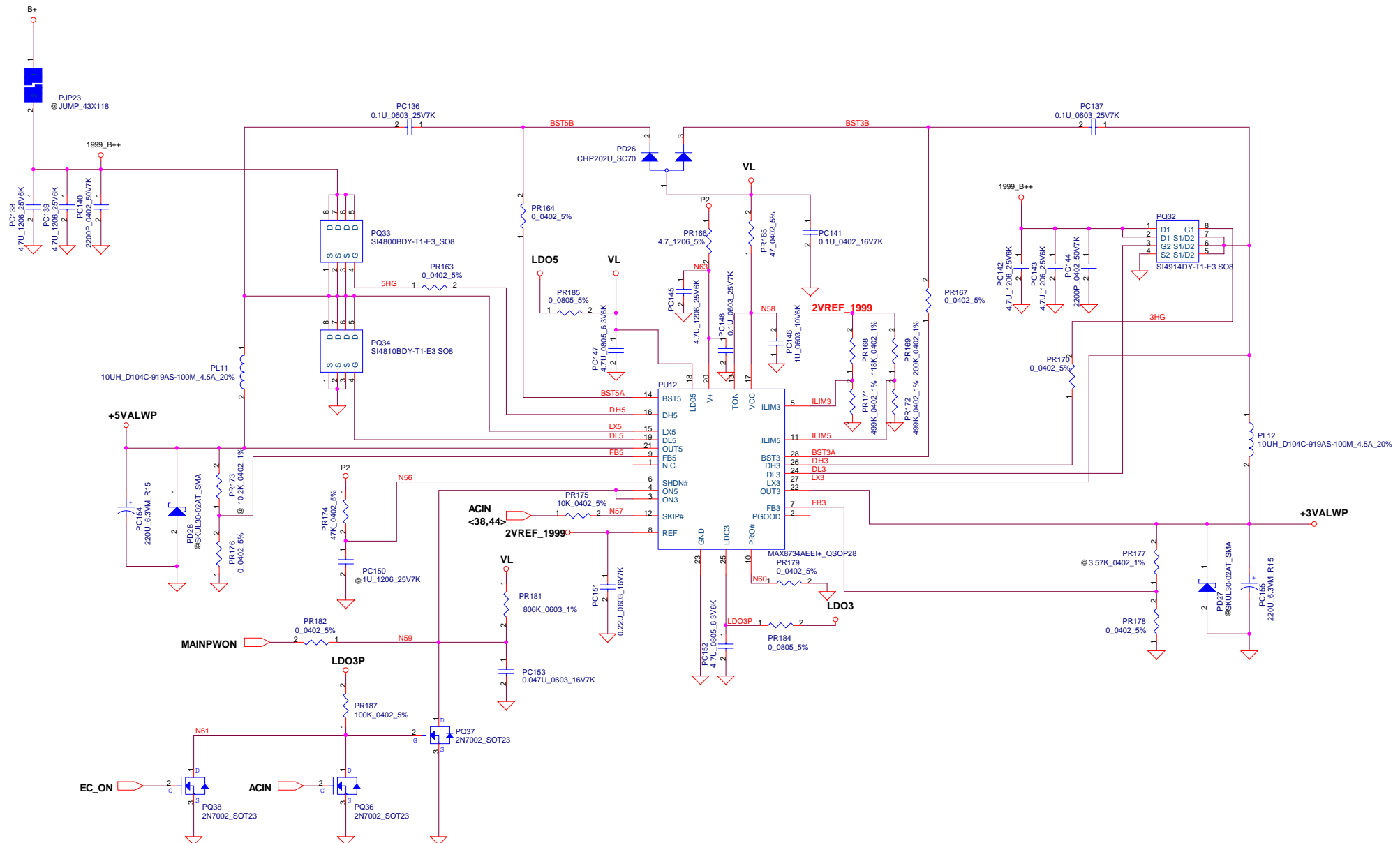
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Cayenne : PR21=200K
Boxster : PR21=300K
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Security Classification		Compal Secret Data			
Issued Date	2005/03/01	Deciphered Date	2006/03/01	Title DCIN / Precharge	
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				Date:	Tuesday, August 30, 2005
				Sheet	43 of 53

Charger

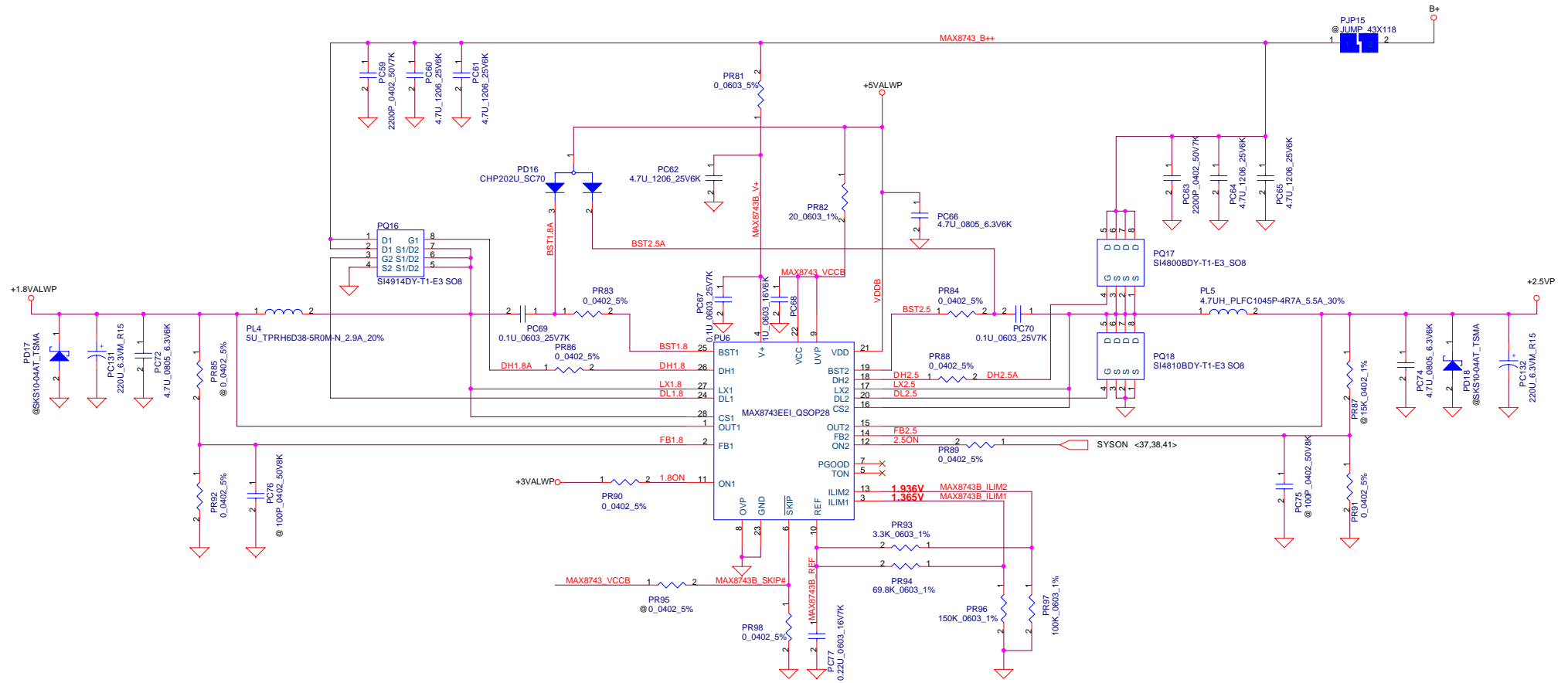


+3VALWP/+5VALWP



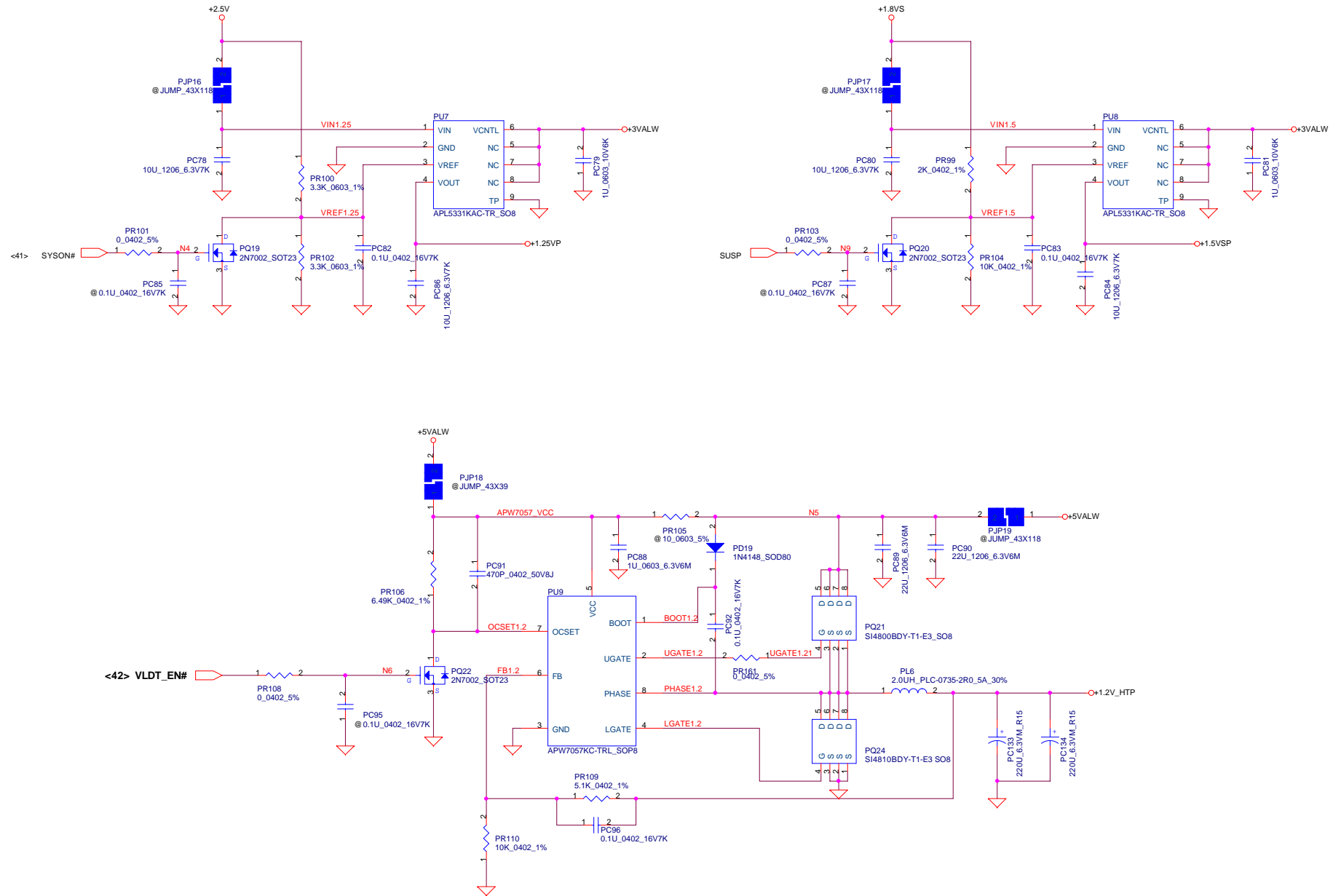
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								Size	Document Number			Rev
								Custom	LA-2771			0.8
								Date:	Tuesday, August 30, 2005			Sheet
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+1.8VALWP/+2.5VP



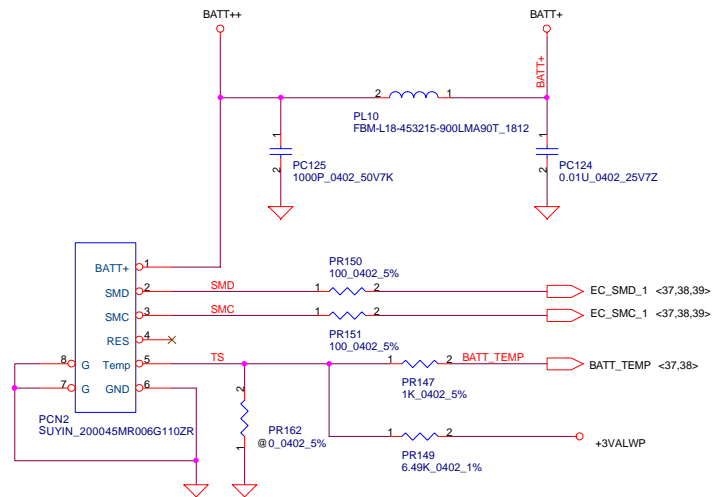
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						Size		Document Number		Rev	
						LA-2771				0.8	
						Date:		Tuesday, August 30, 2005		Sheet 46 of 53	

+1.2V_HTP/+1.5VSP/+1.25VP



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								Size	Document Number						Rev
								Custor	LA-2771						0.8
								Date:	Tuesday, August 30, 2005				Sheet	47	of

Battery Connect/OTP

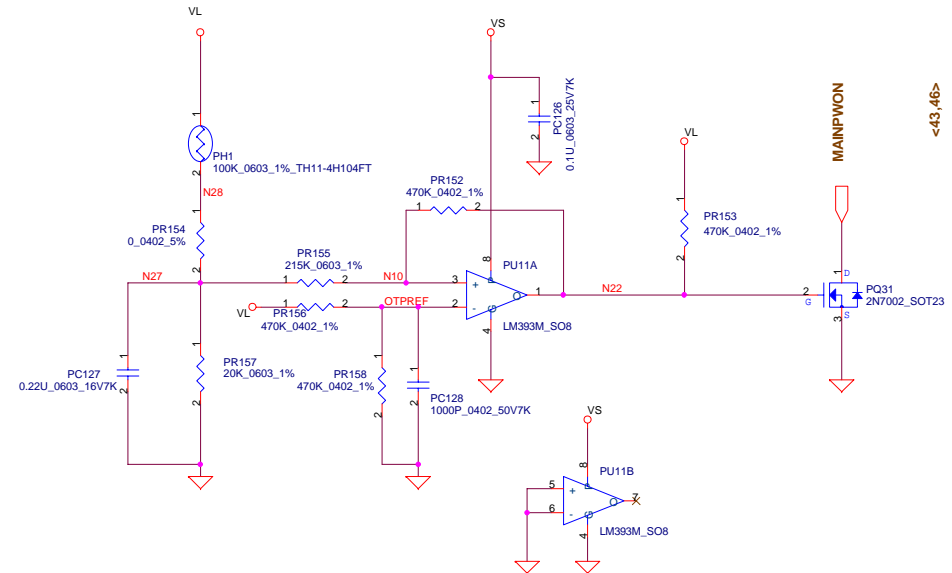


PJPB1 battery connector

SMART Battery:
 1.BATT+
 2.SMBD
 3.SMBC
 4.Res
 5.Temp
 6.GND

CPU

PH1 under CPU botten side :
 CPU thermal protection at 90 +-3 degree C
 Recovery at 50 +-3 degree C



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Version change list (P.I.R. List)

Power section

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Item	Reason for change	PG#	Modify List	Date	B.Ver#
1	Add the functionality to turn on the system on from Off and S4 with the consumer IR.	45	Change 3/5VALWP regulator from MAX1902 to MAX1999	2005.04.08	
2	Change PCN1 from SP020022200 to SP020024800.	49	Change PCN1 from SP02000AO00 to DC040001P00.	2005.04.08	
3	Because EMI test fail	48	Change CPU_CORE HI-SIDE MOS from AO4408 to FDS6294, LOW-SIDE from AO4410 to FDS6676AS	2005.05.18	
4	Because V_bat to Calgary havn a leakage current, cause precharge can't finisn.	44	Add PD30 and PD31 to supply the V_bat power.	2005.06.09	
5	Add air-adapter detector	44	Add PU4 to detector air-adapter in.	2005.07.02	
6	Adjust the MB3887 CC to CP response cause the adapter OCP.	44	Change the PR31 from 100k_0402_1% to 10k_0402_1% Change the PR34 from 10k_0402_1% to 2.74k_0402_1% Change the PC21 from 4700p_0603_50V to 0.01u_0603_50v	2005.07.29	

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I tem	Fixed Issue	Reason for change	PAGE	Modify List	M.B. Ver.
<2005.04.18>	1	HP Jack + SPDIF change type	31 , 33	Del : U27 , C563 , C564 Add: Q52 , Q53 , Q54 , Q56 , Q57 , R571 , C730 , C731 , R567 , R569 , R568 , R570	0.2
	2	Support CIR wake up from battery mode	4 , 37 , 38 , 41 , 35	12VALW change to B+ +3VALW change to LDO3 , +5VALW change to LDO5	0.2
	3	for Marvell express card Rest timing	20 , 28	Add: Q55	0.2
	4	for some HDD's LED alway on	24	Del: D29 , R259 , Q10	0.2
	5	for card bus can't work	27	S1_VCC and S1_VPP change to +S1_VCC and +S1_VPP	0.2
	6	For nissan common design	35	JP28 and JP29 pin swap	0.2
	7	For keyboard issue	37	Del: D27	0.2
<2005.04.27>	1	wake up from LAN	38	Add: R575(Pull UP PME_EC#)	0.3
	2	For VOL_UP,DOWN function issue	38	POP: R418,R419,R420,R421	0.3
<2005.05.3>	1	For CIR wake up	38	Add: R576, R577 to option	0.3
<2005.05.4>	1	EC 910L include portion circuit	39	Add: R578 , Del:C630 , R422 , Q22 , U35A	0.3
	2	ME change LED type	36	D18,D20,D21 from right angle change to vertical type	0.3
<2005.05.6>	1	Add wireless LED current limit resister	17	Add: R581 current limit resister	0.3
<2005.05.9>	1	TP conn pin reverse	35	Pin swap	
<2005.05.10>	1	ME change LED type	36	D25 from right angle change to vertical type	
	2	HP requirement from 75 ohm change to 33 ohm	33	R567 , R569 from 75 ohm change to 33 ohm	
	3	For nissan common design	35	Add: R582 , R583	
<2005.05.11>	1	For 2 way and 4 way touch pad	36	Add: R584 , R585	
<2005.06.10>		update JP23 dual USB connector to reverse type			0.4
		DFX modification for Rev0.4 MB			
		Change MR954, MC928, MR924, MR922, MR932, MC944, MC970, MC976, MC978, MC926 to correct pad size with Compal layout rule			
		update USB connector to reverse type			
		Change D6 form RB411 to RB491			

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<2005.08.11>

<2005.08.23>

Item	Fixed Issue	Reason for change	PAGE	Modify List	M.B. Ver.
1		Delect all reserve 0 ohm resistors.	41	Delete R24, R125, R21 , R73 , R263, R565	0.5
2		For EMI solution on switch connector	11	Add C753~C771 total 19 pcs	0.5
3		For ATI suggestion on RS480	14	Change C200, C202, C242, C232 from 0.1U 16V4Z 0402 to 1U 6.3V4K 0402	0.5
4		Relocate damping resistor to solve Sandisk issue	26	Relocate R266, R458, R459, R460, R461, R462	0.8
5		Change from AGND to DGND for Codec precision improvement	31	Change Q16/Q17 pin3 and R334 pin2 to DGND	0.8
6		Add +3VALW power rail for Boxster lid switch use	35	Add +3VALW to JP28 pin25	0.8
7		Reserve C700, for soft start if necessary	31	Reserve C700	0.8
8		Reserve R600 M_SEN#, currently this signal isn't used	38	Reserve R600	0.8
1					
2					
1					
2					
3					
1					
2					
1					
2					
3					
4					
1					
2					

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